KEYSIGHT

Accelerating High-Speed Digital Design Workflow with Keysight ADS

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Solution Engineer

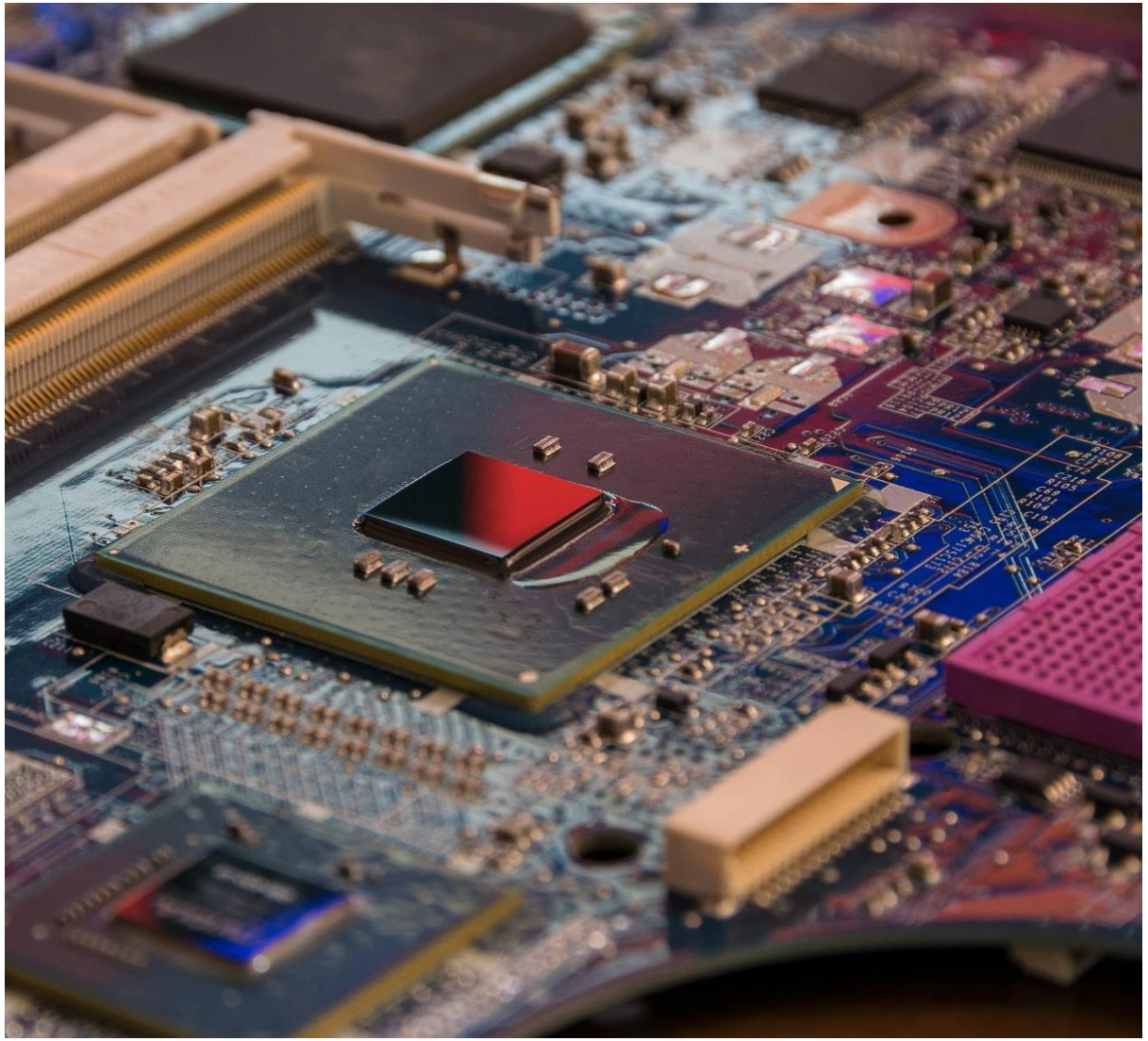
Agenda

- Keysight Advanced Design System Software – High Speed Digital Solutions
- ADS Memory Design Workflow – Memory Designer
- ADS SerDes Design Workflow – System Designer for PCIe®
- Conclusion

High Speed Digital Designs Are Already Complex!

The challenge of today's hardware designer

- Design margins continue to shrink and speed increases, there is less room for error in your design
- Hard to collate results, gather insights into the design and optimize the design
- After a small production run, it can be difficult to troubleshoot issues found
- Uncertainty for product reliability leads to significant risk to design schedules
- Hours of setup time before the first simulation
- Topology and configuration changes require multiple schematics and many parameter values to sweep through

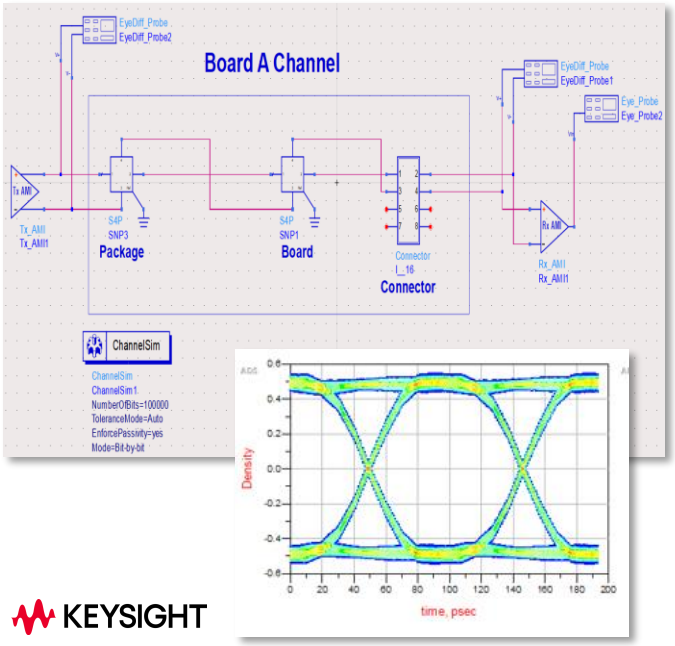


ADS HSD Design Flow

ADS accelerate High-Speed Digital Workflows

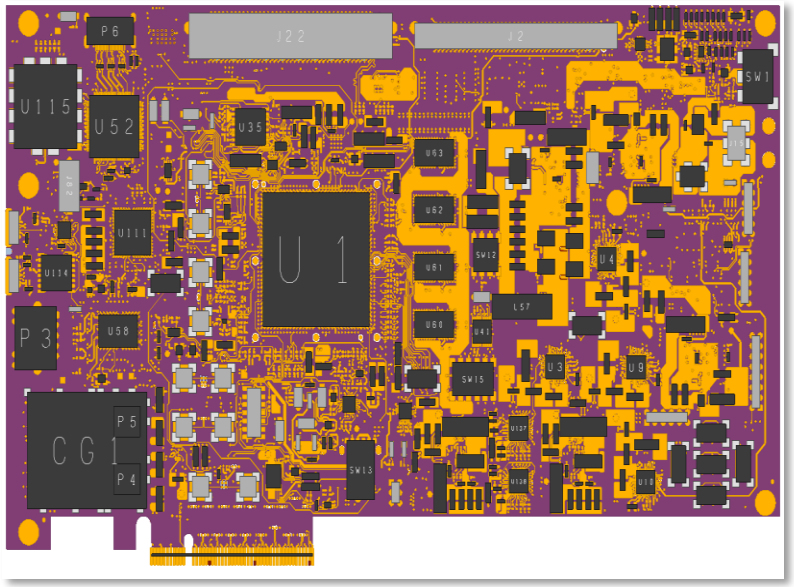
Pre-Layout

Pre-investigation of channel performance



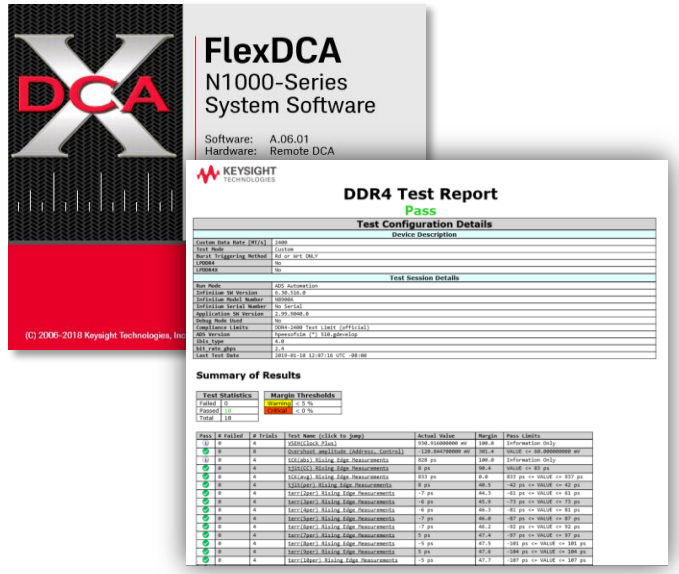
Post-Layout

EM simulation of Design for Signal and Power Integrity

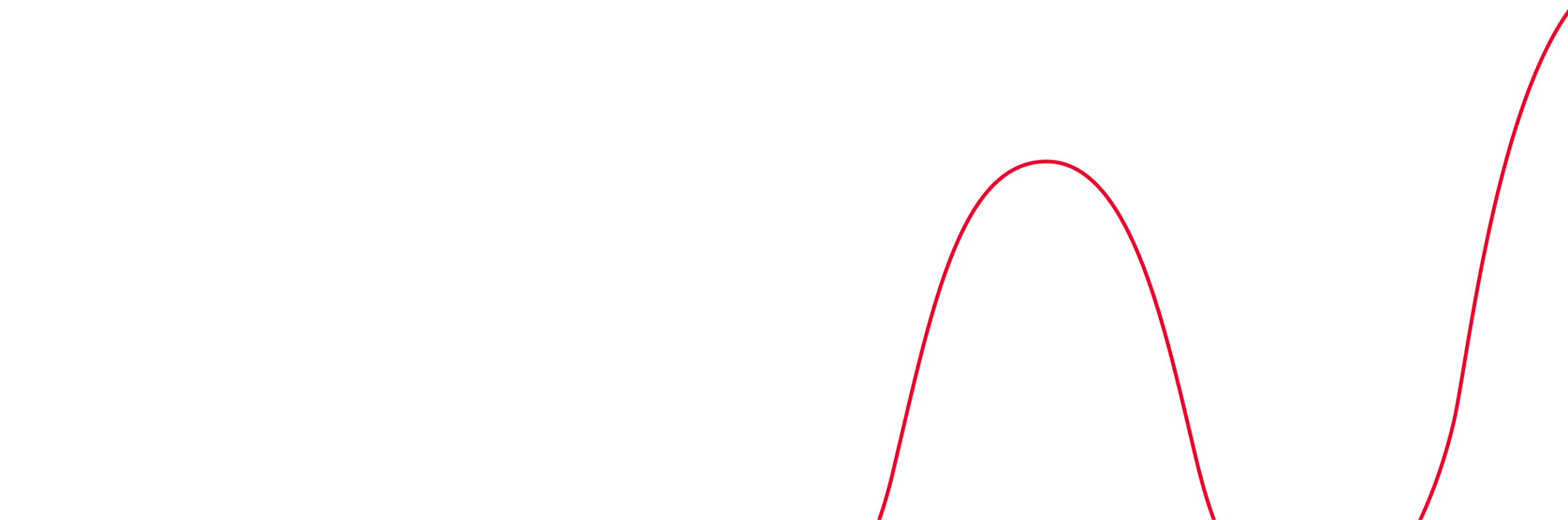


Verification/Measurement

Verification of Design with Compliance Test Benches and Instrument measurements



Memory Design Workflow



What Matters in Memory Simulations?

Simulator, Chipset Models, Channel models

<u>For TX and RX</u>

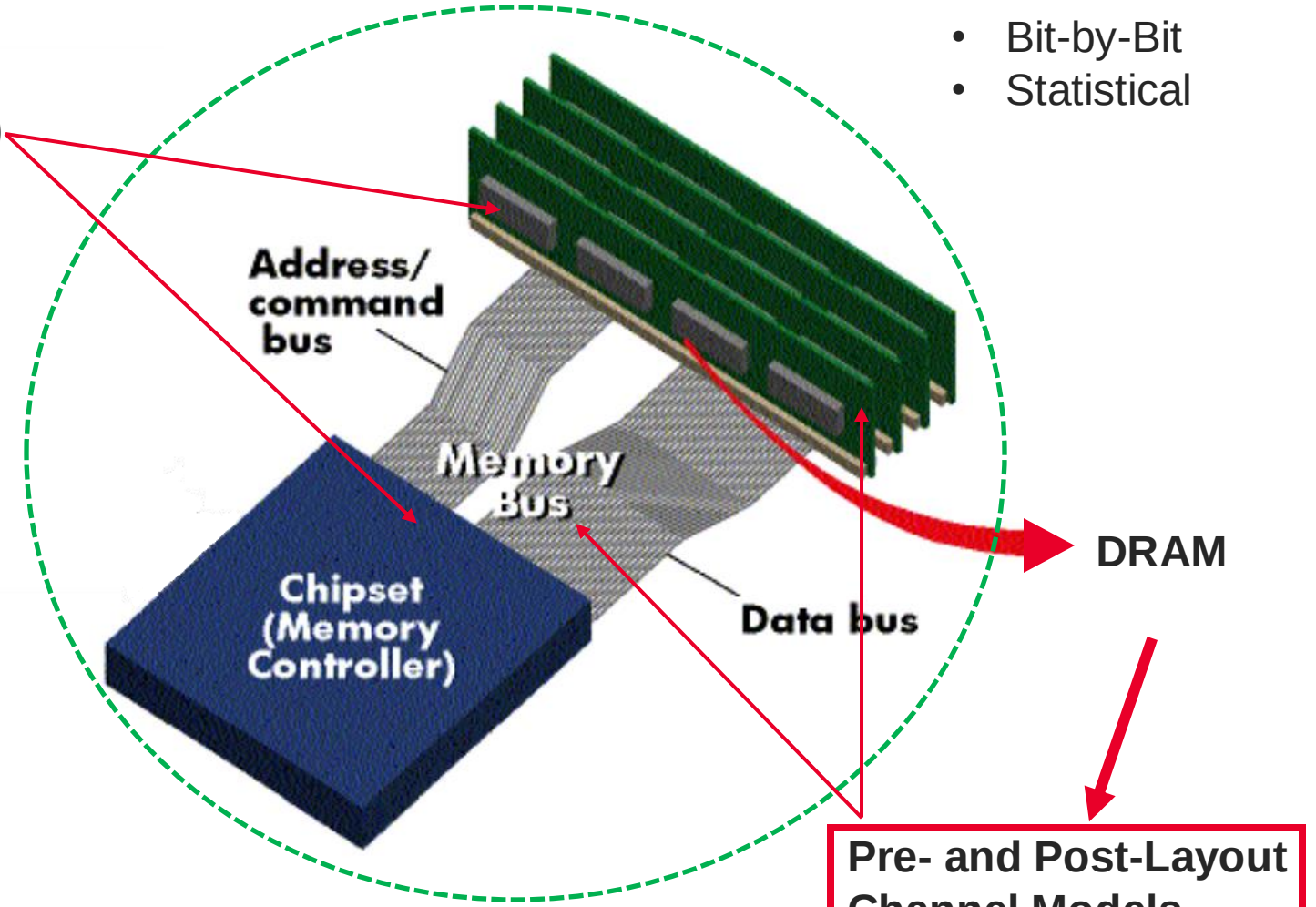
IBIS Models
(Input/Output Buffer Information)

IBIS-AMI Models
(Algorithmic Modeling Interface)

HSPICE Models

Simulation Technologies:

- Transient Convolution
- DDR Bus Sim
  - Bit-by-Bit
  - Statistical



What Are Typical Methods Used for Modeling the Channels?

System Design (Pre-Layout) Workflow vs. Verification (Post-Layout) Workflow

System Design - Pre-Layout Workflow (no layout is done…)

- Rule of thumb
- Equation-based circuit models
- Static cross-sectional models
- Quasi-static electro-magnetic models
- …

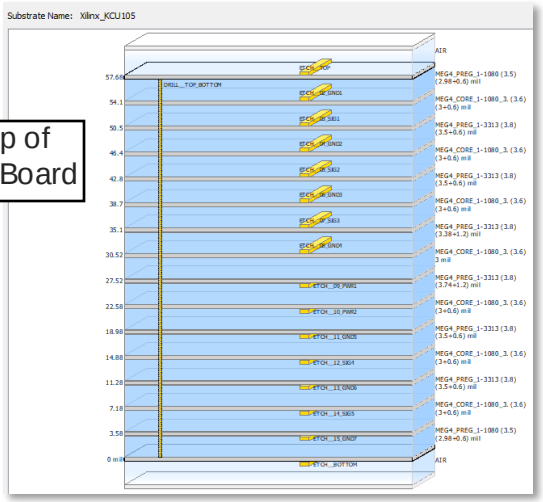
- Hybrid EM solvers

- Full-wave 3D electro-magnetic models
  - FEM, FDTD, FIT, MoM, etc.
- …

Verification - Post-Layout (layout is done and available)

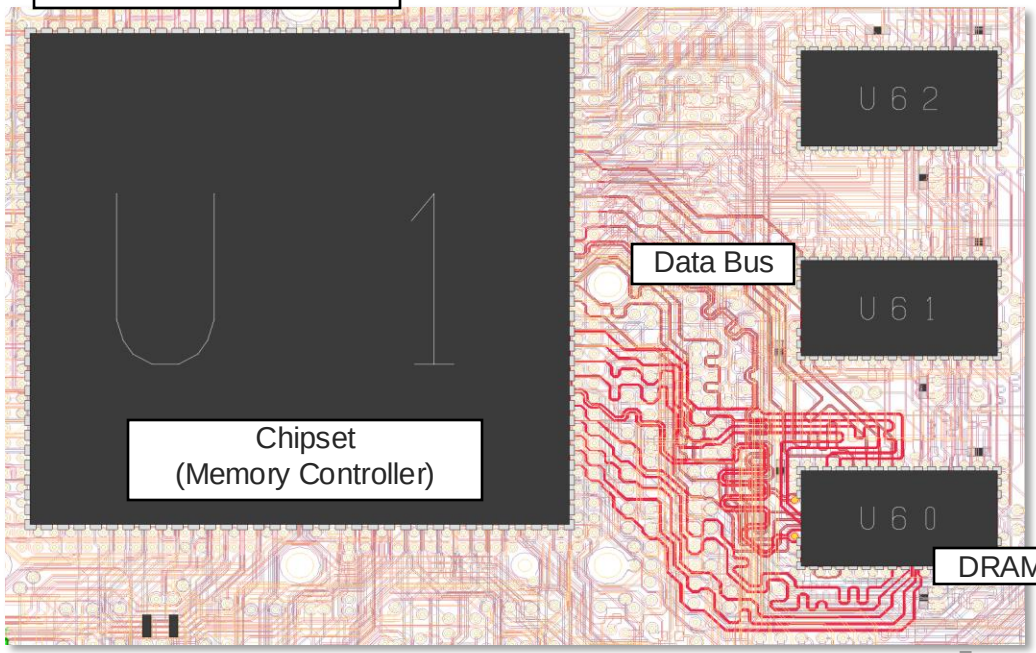
Speed

Accuracy



Substrate stack-up of High-Speed Digital Board

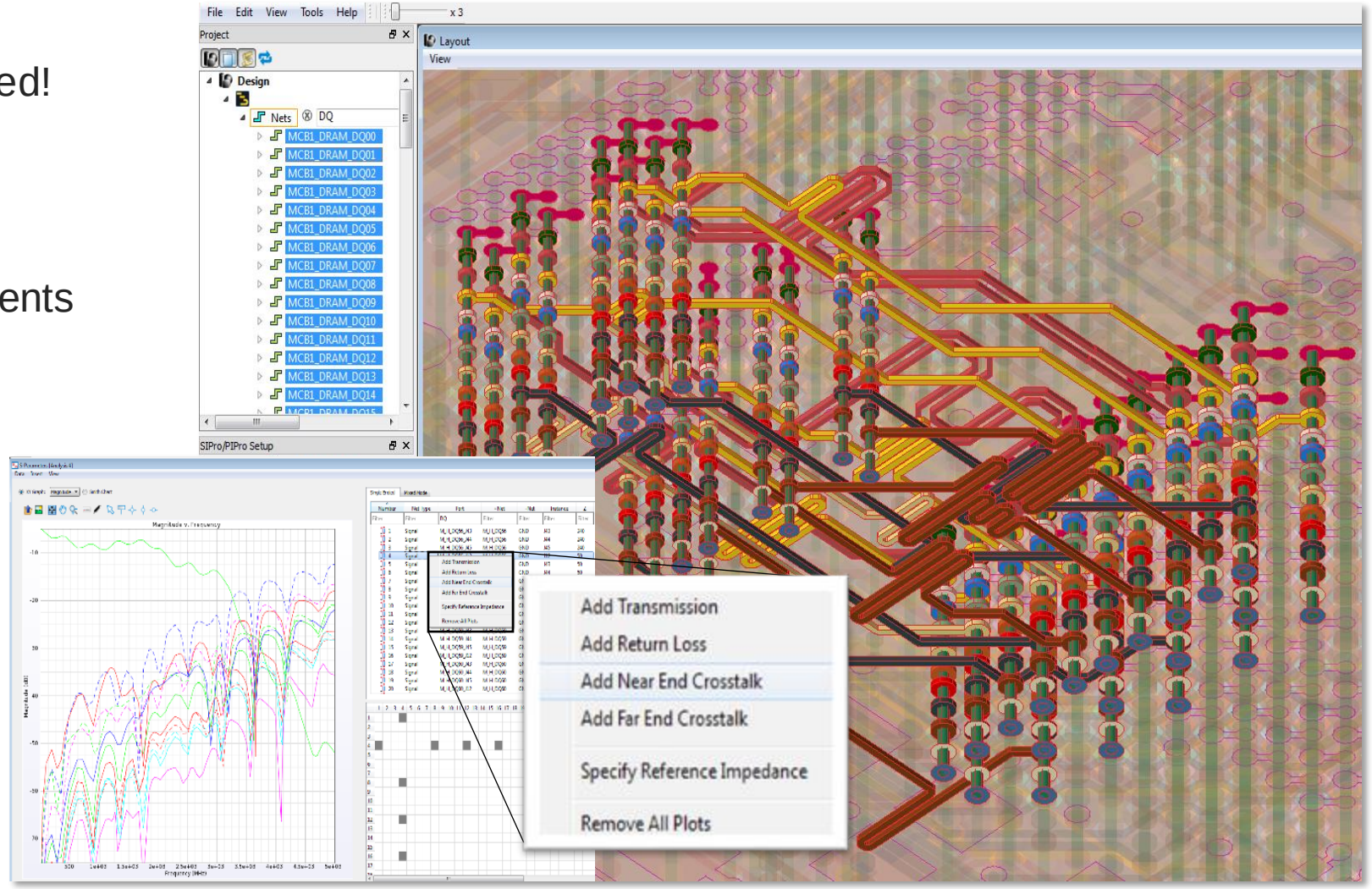
High-Speed Digital Board for Simulation (only showing on Memory)



SIPro Electromagnetic PCB Extraction

Layout to results in less than 20 clicks

- No layout simplification required!
- Net-driven
- Guided port creation
- Quickly plot all crosstalk elements from the same component
- Easily plot TDR/TDT
- Mixed-mode S-parameters
- One-click schematic generation



How SIPro Performs *(Fast & Accurate)* Analysis?

Hybrid Approach – FEM + Momentum

SIPro Analysis of **DDR_DQ4** Net

Variation along Z-axis:
FEM Domain

Variation along Z-axis:
FEM Domain

No Variation along Z-axis:
Momentum Domain

Key Takeaway

Keysight SIPro EM-Hybrid approach provides faster simulation results while maintain good accuracy as compared to traditional FEM EM engines

What Matters in Memory Simulations?

Simulator, Chipset Models, Channel models

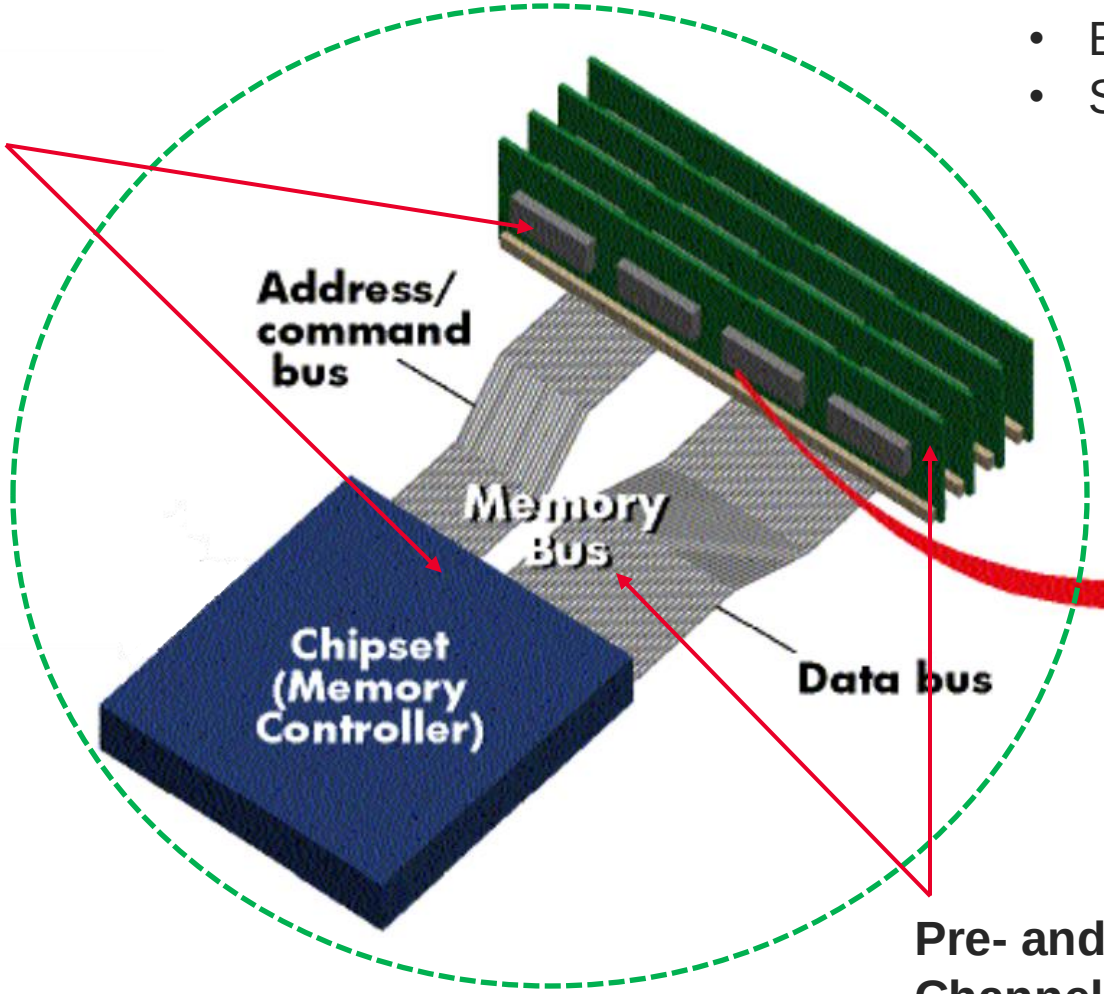
For Controller and DRAM

IBIS Models
(Input/Output Buffer Information)

IBIS-AMI Models
(Algorithmic Modeling Interface)

HSPICE Models

Simulation Technologies:
- Transient Convolution
- DDR Bus Sim
  - Bit-by-Bit
  - Statistical



Pre- and Post-Layout Channel Models

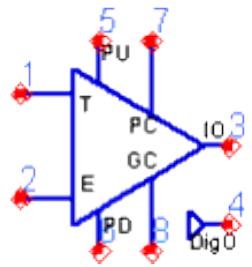
IBIS: Input/output Buffer Information Specification

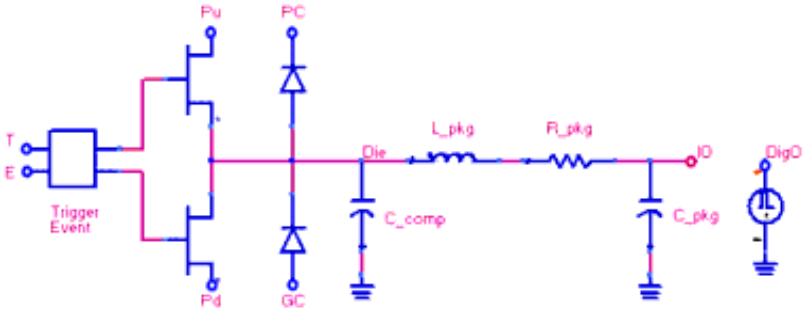
- IBIS is an industry-standard model for characterizing inputs and outputs of Integrated Circuits
- Supplied in a data file written in text format (.ibs)
- Only the operation of the IO buffer is described
- Primary use for designing chip-to-chip serial links like Memory Modules and Boards.
- In digital circuits, from the viewpoint that it is good to consider the effects of reflection and crosstalk, a solution is sought based on the characteristic impedance of the IO buffer and wiring (reflection analysis method)
- IBIS Open Forum
  - http://www.eda-stds.org/ibis/
- IBIS 5.0 was approved in August 2008, and an Algorithmic Modeling Interface (AMI) was added to the existing specification

IBIS model

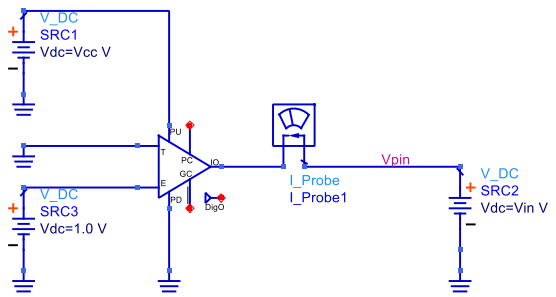
Example

- Pullup, Pulldown, Protection Diode Power Clamp, Ground Clamp, Die Capacitance (C_comp) and Package RLC

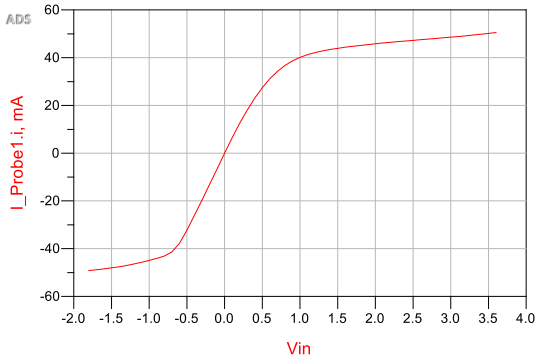




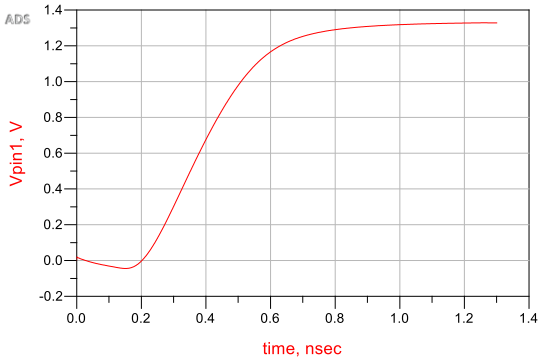

```
[Model] IO_40
Model_type I/O

C_comp          0.4pF       0.39pF       0.41pF
Vinl =    0.1V
Vinh =    0.2V
|
[Temperature Range]    25.0000       120.0000       0.0
[Voltage Range]        0.3V          0.27V          0.37V
[Pulldown]
|Voltage      I(typ)        I(min)        I(max)
-0.8V        -20mA    -20mA    -20mA
-0.4V        -10mA    -10mA    -10mA
0V            0.0mA    0.0mA    0.0mA
0.4V          10mA     10mA     10mA
0.8V          20mA     20mA     20mA
|
[Pullup]
|Voltage      I(typ)        I(min)        I(max)
-0.8V         20mA     20mA     20mA
-0.4V         10mA     10mA     10mA
0V            0.0mA    0.0mA    0.0mA
0.4V         -10mA    -10mA    -10mA
0.8V         -20mA    -20mA    -20mA
|
[GND_clamp]
|Voltage       I(typ)          I(min)          I(max)
-1.2V          -2mA            -2mA            -2mA
-0.2V          0.0A            0.0A            0.0A
0.0V           0.0A            0.0A            0.0A
1.2000V        0.0A            0.0A            0.0A
|
[POWER_clamp]
|Voltage       I(typ)          I(min)          I(max)
-1.2V          2mA             2mA             2mA
-0.2V          0.0A            0.0A            0.0A
0.0V           0.0A            0.0A            0.0A
1.2000V        0.0A            0.0A            0.0A
|
[ISSO PD]
|Voltage       I(typ)          I(min)          I(max)
-0.2700V        15.0mA           13.5mA           18.5mA
0.2700V         0.0mA            0.0mA            0.0mA
0.3700V         0.0mA            0.0mA            0.0mA
|
[ISSO PU]
|Voltage       I(typ)          I(min)          I(max)
-0.2700V        -15.0mA          -13.5mA          -18.5mA
0.2700V         0.0mA            0.0mA            0.0mA
0.3700V         0.0mA            0.0mA            0.0mA
```



Pulldown



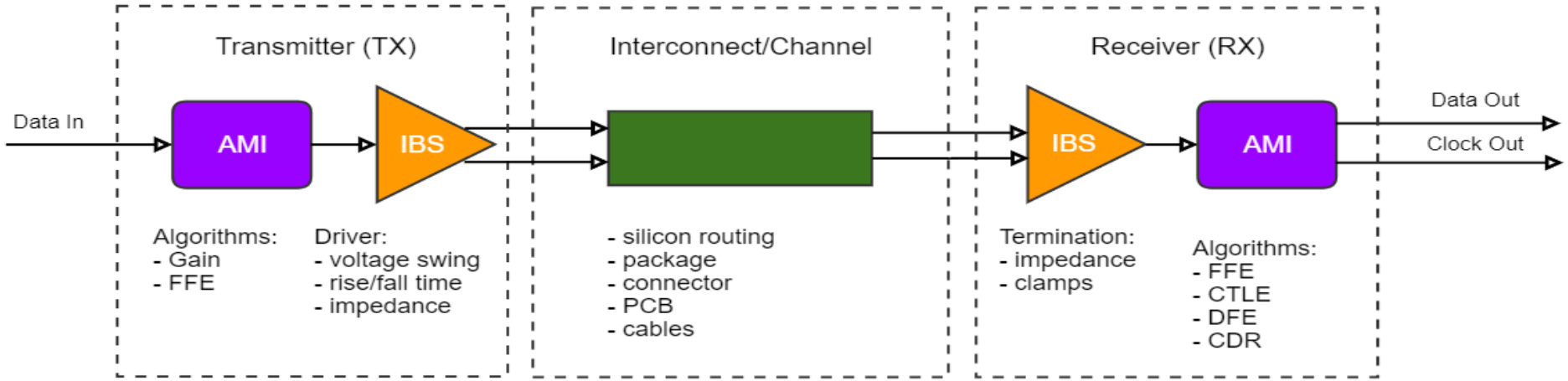
Rising Waveform



Overview of IBIS-AMI Models

Algorithmic Modeling Interface (AMI)

- Modeling interface for Memory/SerDes behavioural Models – such as Equalization and Clock Data Recovery (CDR)
- Added alongside with traditional IBIS flow in IBIS version 5.0
- Acts as a Digital Signal Processing block – takes input signal waveform and outputs a modified waveform
- Developed by SerDes vendors to match and represent the actual chip behaviour

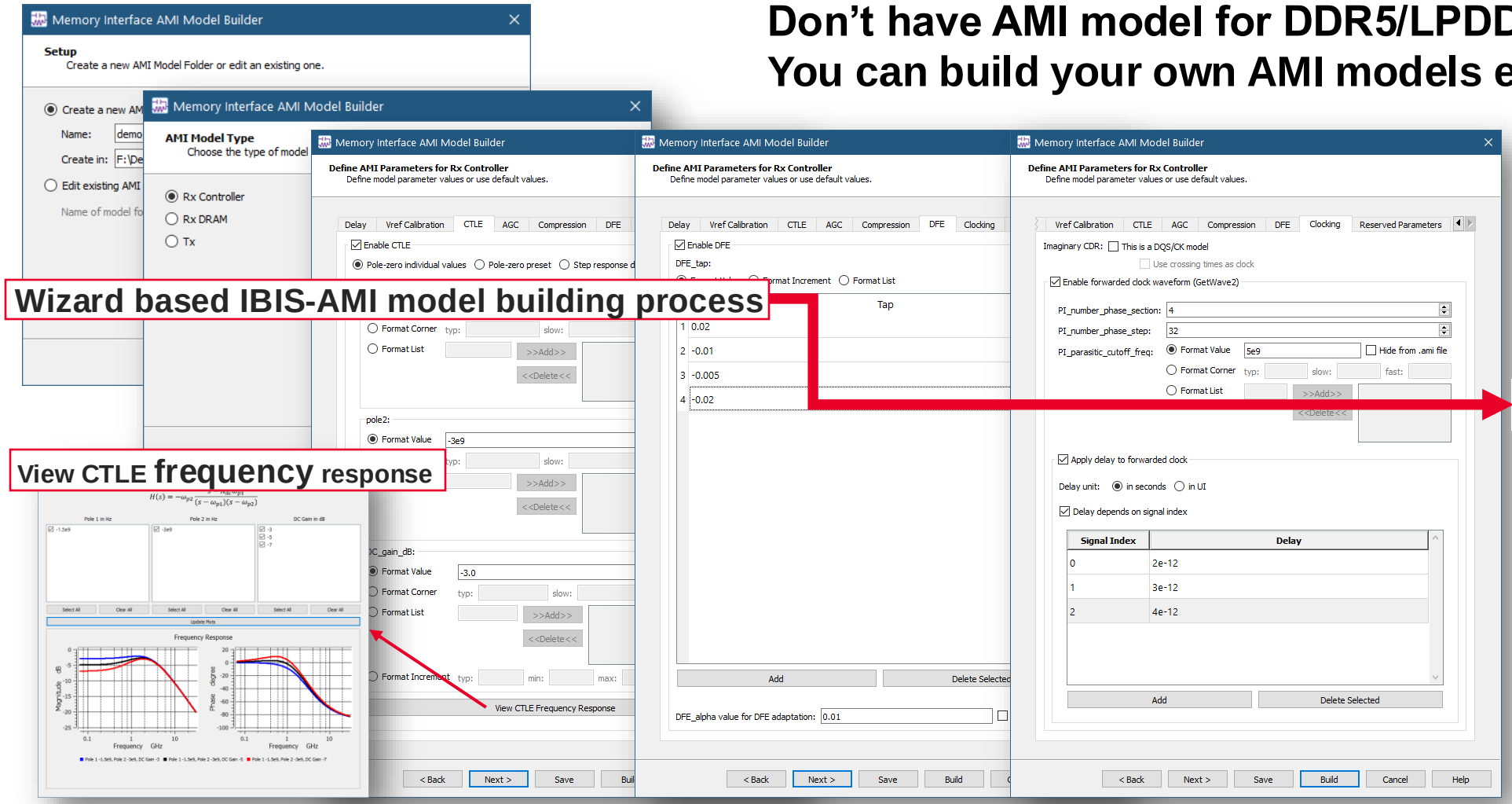


Memory Interface IBIS-AMI Model Builder

DDR5/LPDDR5 and PAM-n IBIS-AMI Model building wizard

Key Takeaway
Keysight ADS provided quick an easy generation of IBIS-AMI models to kick-start your simulation

Don’t have AMI model for DDR5/LPDDR5? No problem!
You can build your own AMI models easily and quickly!



Wizard based IBIS-AMI model building process

View CTLE frequency response

Build

- .ami
- .dll or .so
- .ibs
- .conf (re-usable)

Extensive standard model features:

- **Delay**
- **Vref Calibration**
- **CTLE**
- **AGC**
- **Compression**
- **DFE**
- **Forward clocking (GetWave2)**
- **…**

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<u>For TX and RX</u>

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IBIS-AMI Models
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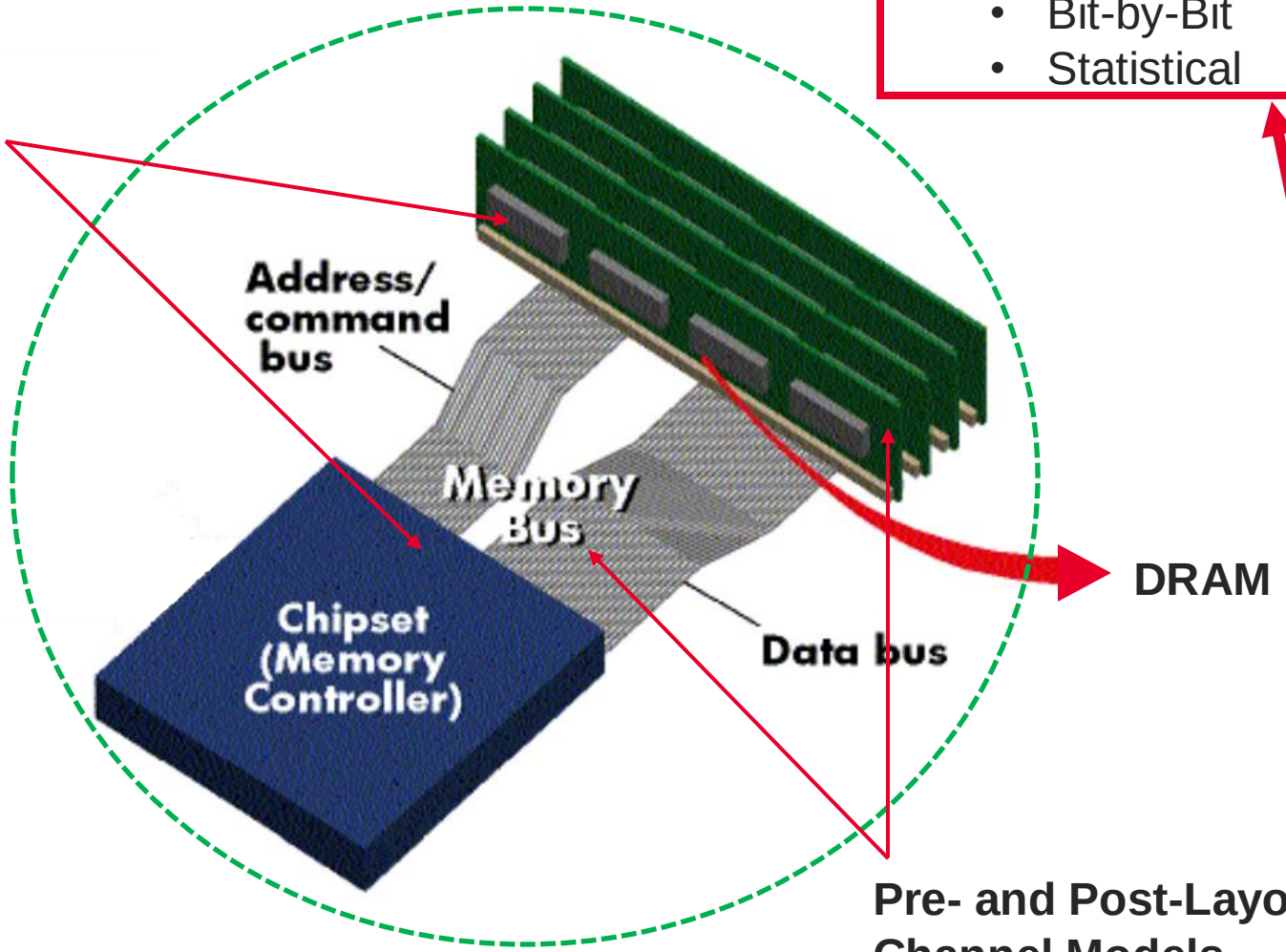
HSPICE Models

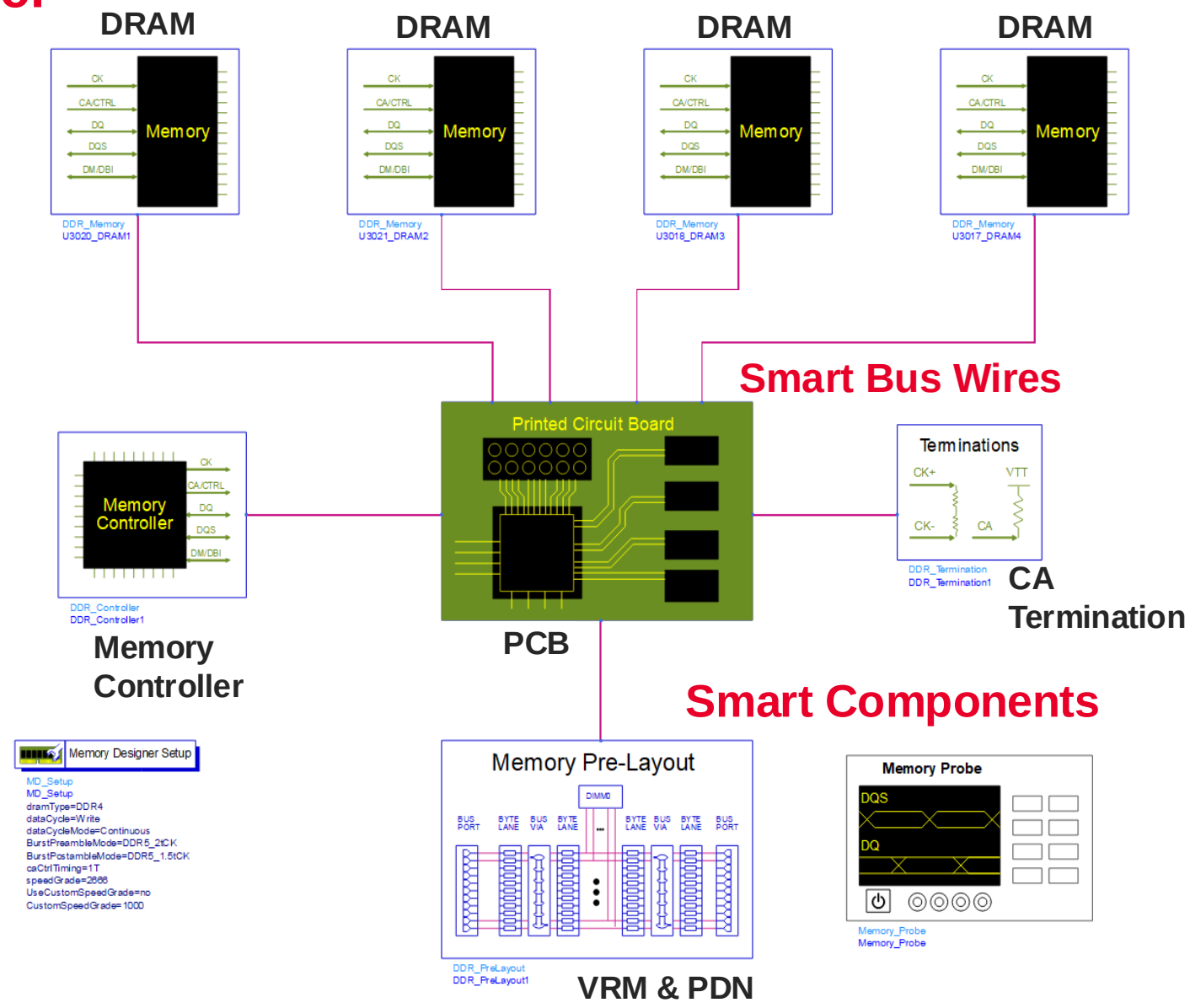


Pre- and Post-Layout Channel Models

PathWave ADS Memory Designer

- Simulation Environment designed with the Memory Design Engineer in mind
- Smart bus, components, and Memory Eye Probe
- Multiple Simulation Engines
  - Transient Convolution
  - DDR BUS Sim
    - Bit-by-Bit Simulation
    - Statistical Simulation
- Compliance Report Generation
- Single-Ended PAM-4 simulation capability
- IBIS-AMI model generation wizard
- CA Data Bus Designer
- DDR extraction wizard in SIPro

and much more…

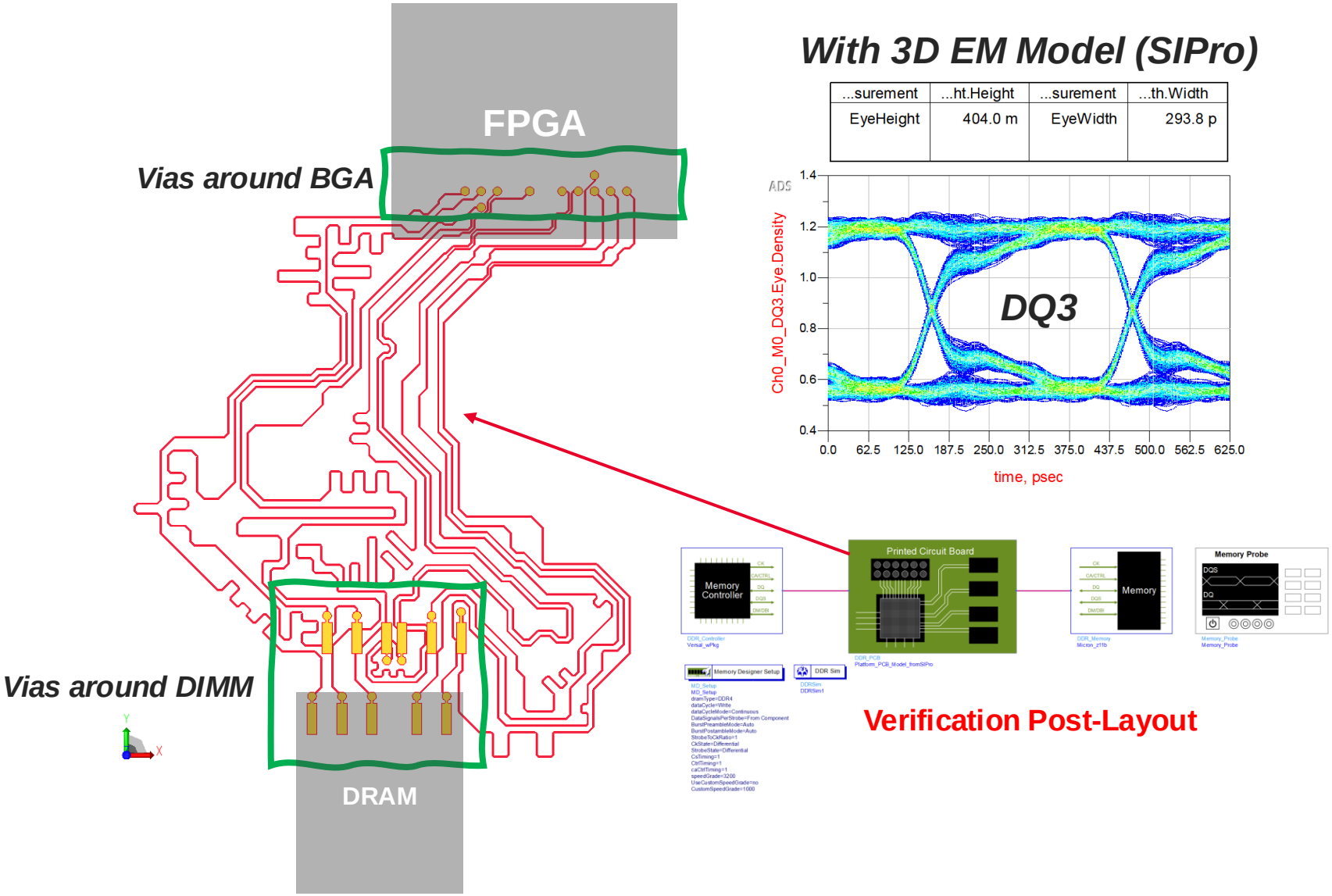


Key Takeaway

Smart workflow to be efficient in your design setup and simulation results analysis

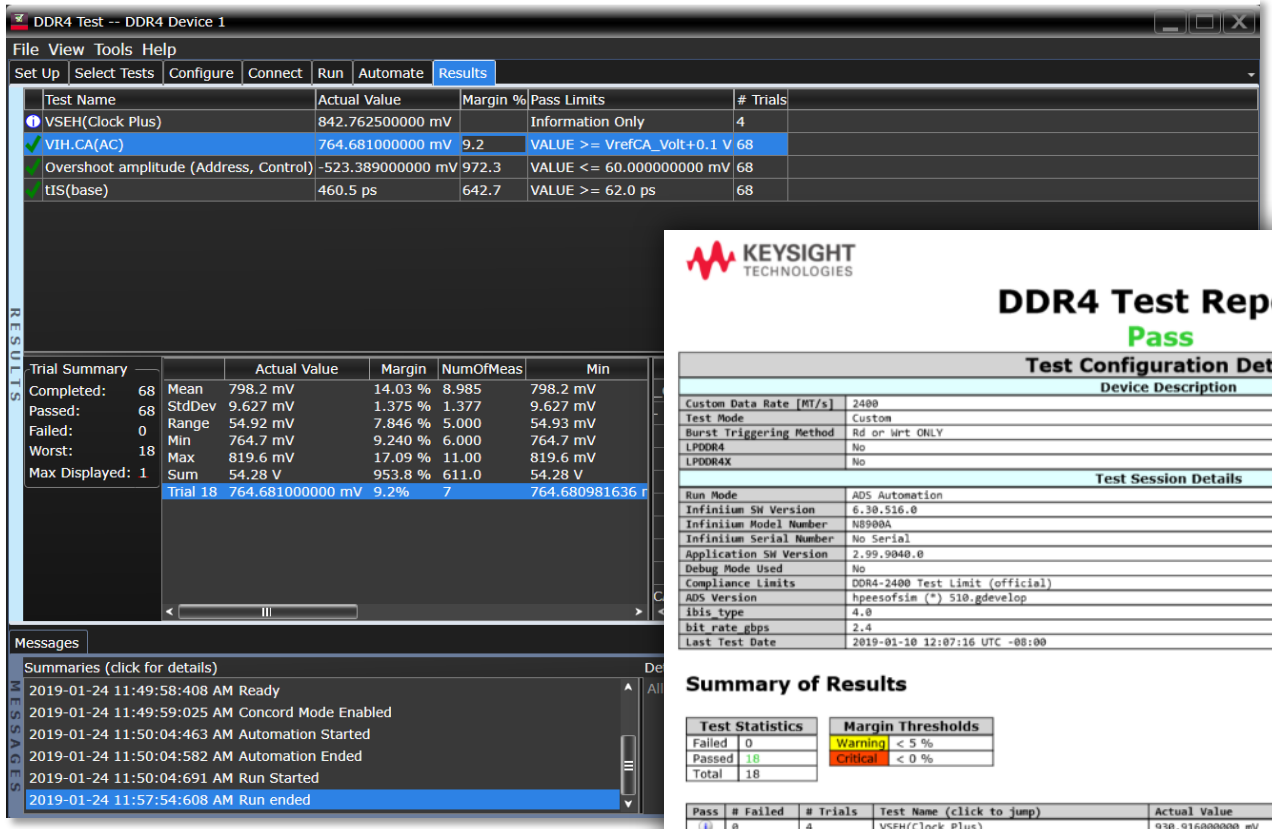
Example – Byte1 (DQ0~DQ7,DQS0 and DM0) on Platform Board

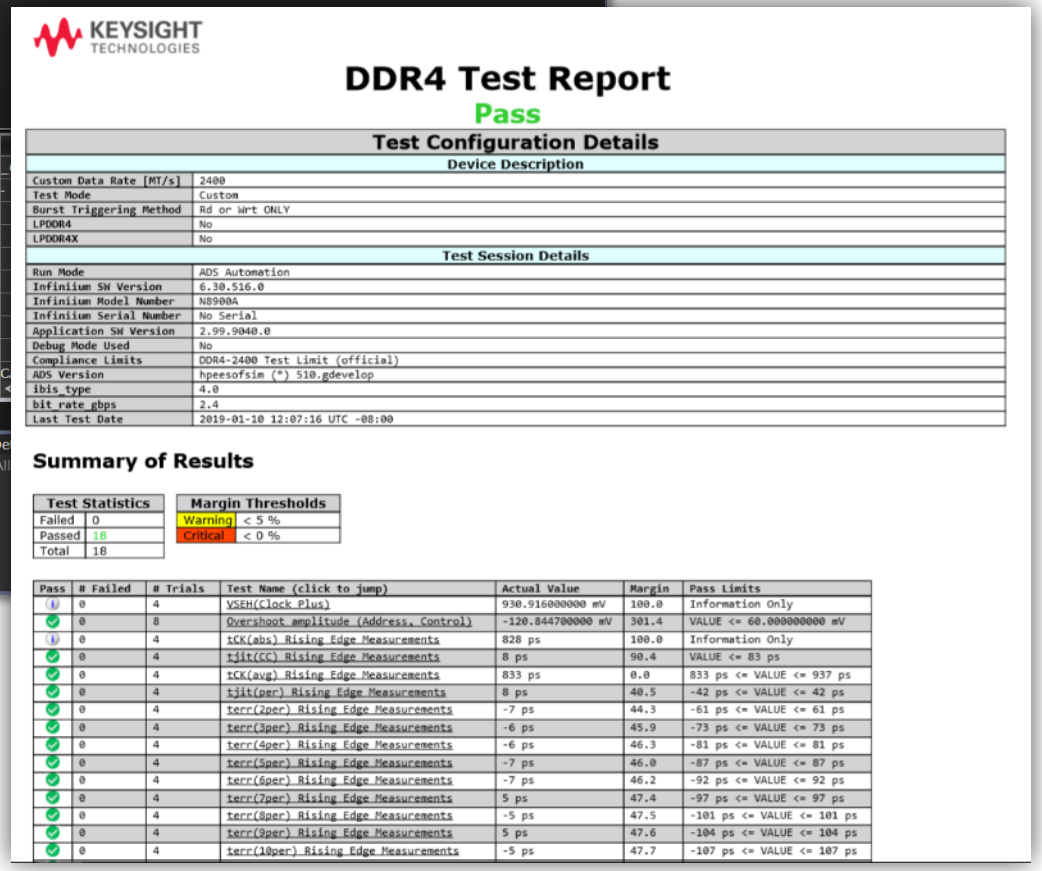
Simulation Structure, Setup, and Results



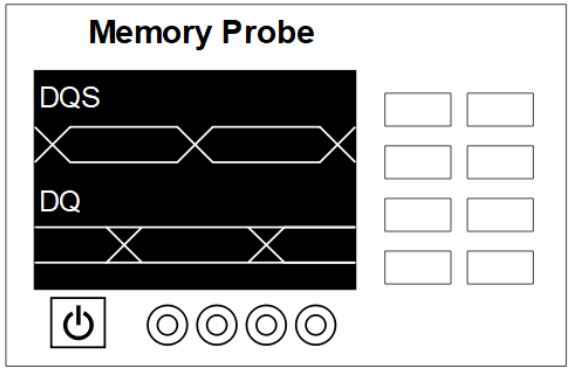
Investigate Pre-Compliance for Sign-Off

Industry proven measurement science

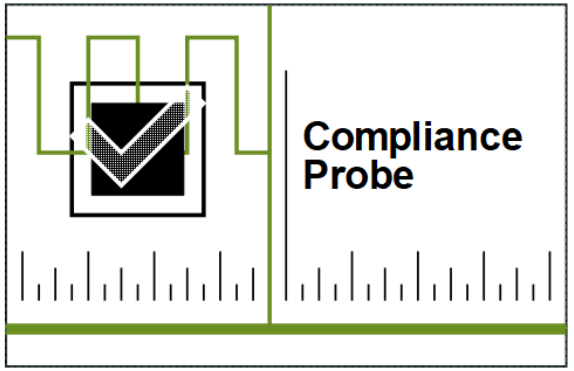




Automatically invoked and controlled by ADS



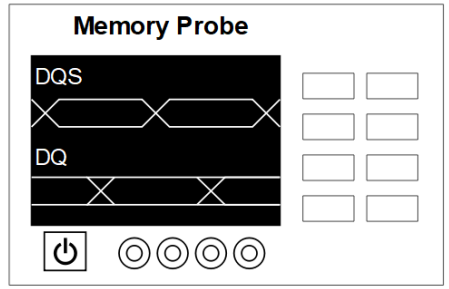
Memory_Probe
Memory_Probe



Compliance_Probe
Compliance_Probe

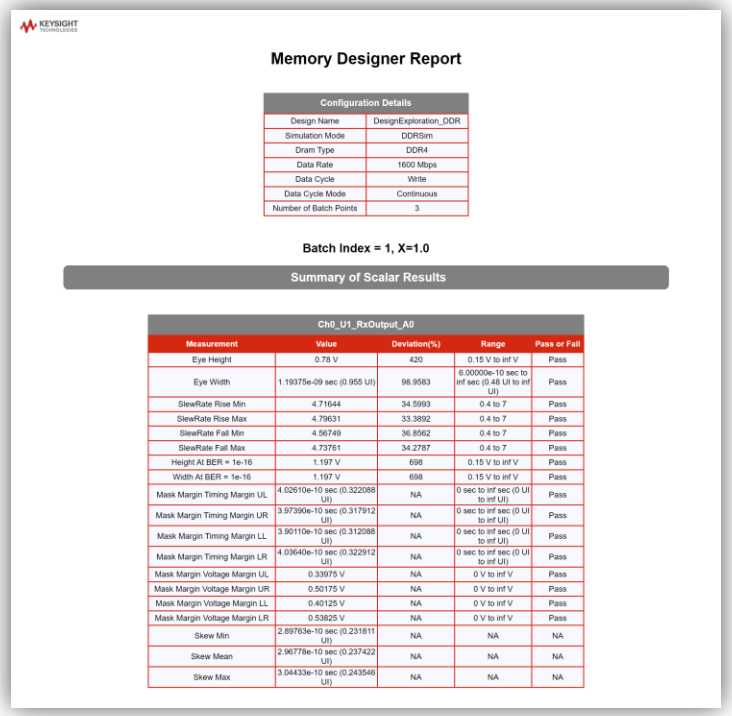
Design Exploration with HTML Report

Pass/Fail & Eye, Waveform, Bathtub plots



Memory_Probe
Memory_Probe

- **Design Exploration** in Memory_Probe now supports HTML report
- Pass/Fail for scalar measurements, otherwise output only plots (eye density, waveform data, bathtub, etc)
- Requires “Datalink” installation



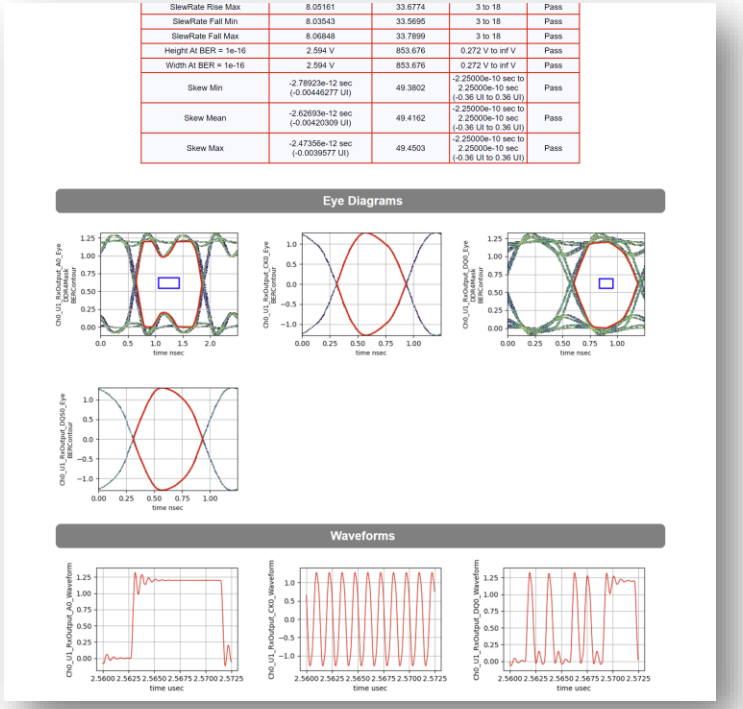
Memory Designer Report

Configuration Details	
Design Name	DesignExploration_DDR
Simulation Mode	DDRSim
Dram Type	DDR4
Data Rate	1600 Mbps
Data Cycle	Write
Data Cycle Mode	Continuous
Number of Batch Points	3

Batch Index = 1, X=1.0

Summary of Scalar Results

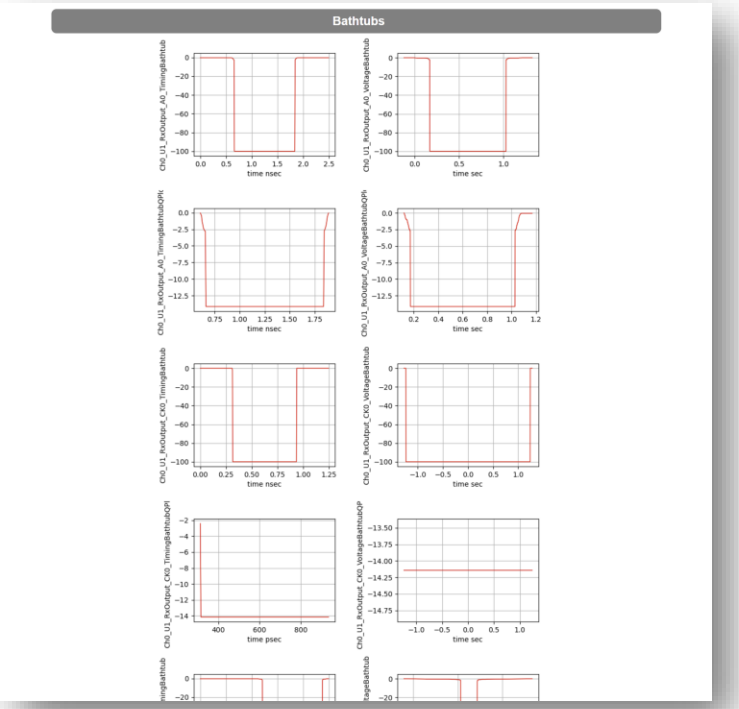
Ch0_U1_RxOutput_A0				
Measurement	Value	Deviation(%)	Range	Pass or Fail
Eye Height	0.78 V	420	0.15 V to inf V	Pass
Eye Width	1.19375e-09 sec (0.955 UI)	98.9583	6.00000e-10 sec to inf sec (0.48 UI to inf UI)	Pass
SlewRate Rise Min	4.71644	34.5993	0.4 to 7	Pass
SlewRate Rise Max	4.79631	33.3892	0.4 to 7	Pass
SlewRate Fall Min	4.56749	36.8562	0.4 to 7	Pass
SlewRate Fall Max	4.73761	34.2787	0.4 to 7	Pass
Height At BER = 1e-16	1.197 V	698	0.15 V to inf V	Pass
Width At BER = 1e-16	1.197 V	698	0.15 V to inf V	Pass
Mask Margin Timing Margin UL	4.02610e-10 sec (0.322088 UI)	NA	0 sec to inf sec (0 UI to inf UI)	Pass
Mask Margin Timing Margin UR	3.97390e-10 sec (0.317912 UI)	NA	0 sec to inf sec (0 UI to inf UI)	Pass
Mask Margin Timing Margin LL	3.90110e-10 sec (0.312088 UI)	NA	0 sec to inf sec (0 UI to inf UI)	Pass
Mask Margin Timing Margin LR	4.03640e-10 sec (0.322912 UI)	NA	0 sec to inf sec (0 UI to inf UI)	Pass
Mask Margin Voltage Margin UL	0.33975 V	NA	0 V to inf V	Pass
Mask Margin Voltage Margin UR	0.50175 V	NA	0 V to inf V	Pass
Mask Margin Voltage Margin LL	0.40125 V	NA	0 V to inf V	Pass
Mask Margin Voltage Margin LR	0.53625 V	NA	0 V to inf V	Pass
Skew Min	2.89763e-10 sec (0.231811 UI)	NA	NA	NA
Skew Mean	2.96778e-10 sec (0.237422 UI)	NA	NA	NA
Skew Max	3.04433e-10 sec (0.243546 UI)	NA	NA	NA



SlewRate Rise Max	8.05161	33.6774	3 to 18	Pass
SlewRate Fall Min	8.03543	33.5695	3 to 18	Pass
SlewRate Fall Max	8.06848	33.7899	3 to 18	Pass
Height At BER = 1e-16	2.594 V	853.676	0.272 V to inf V	Pass
Width At BER = 1e-16	2.594 V	853.676	0.272 V to inf V	Pass
Skew Min	-2.78923e-12 sec (-0.00446277 UI)	49.3802	-2.25000e-10 sec to 2.25000e-10 sec (-0.36 UI to 0.36 UI)	Pass
Skew Mean	-2.62693e-12 sec (-0.00420309 UI)	49.4162	-2.25000e-10 sec to 2.25000e-10 sec (-0.36 UI to 0.36 UI)	Pass
Skew Max	-2.47356e-12 sec (-0.0039577 UI)	49.4503	-2.25000e-10 sec to 2.25000e-10 sec (-0.36 UI to 0.36 UI)	Pass

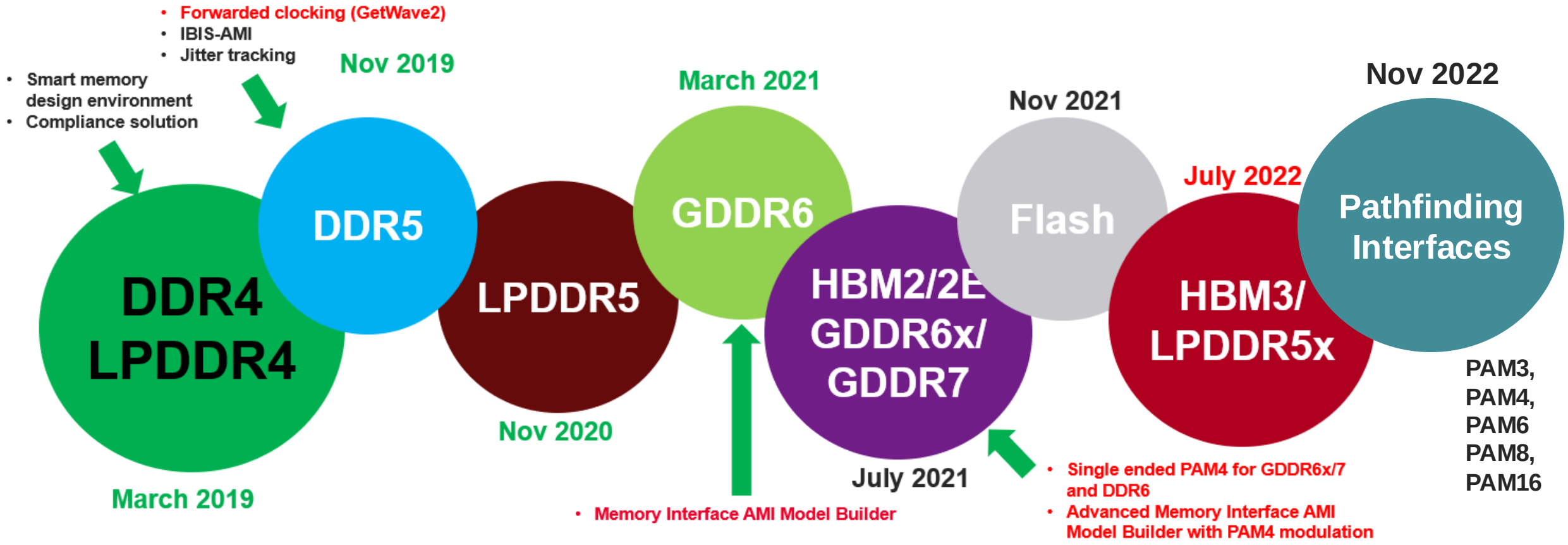
Eye Diagrams

Waveforms



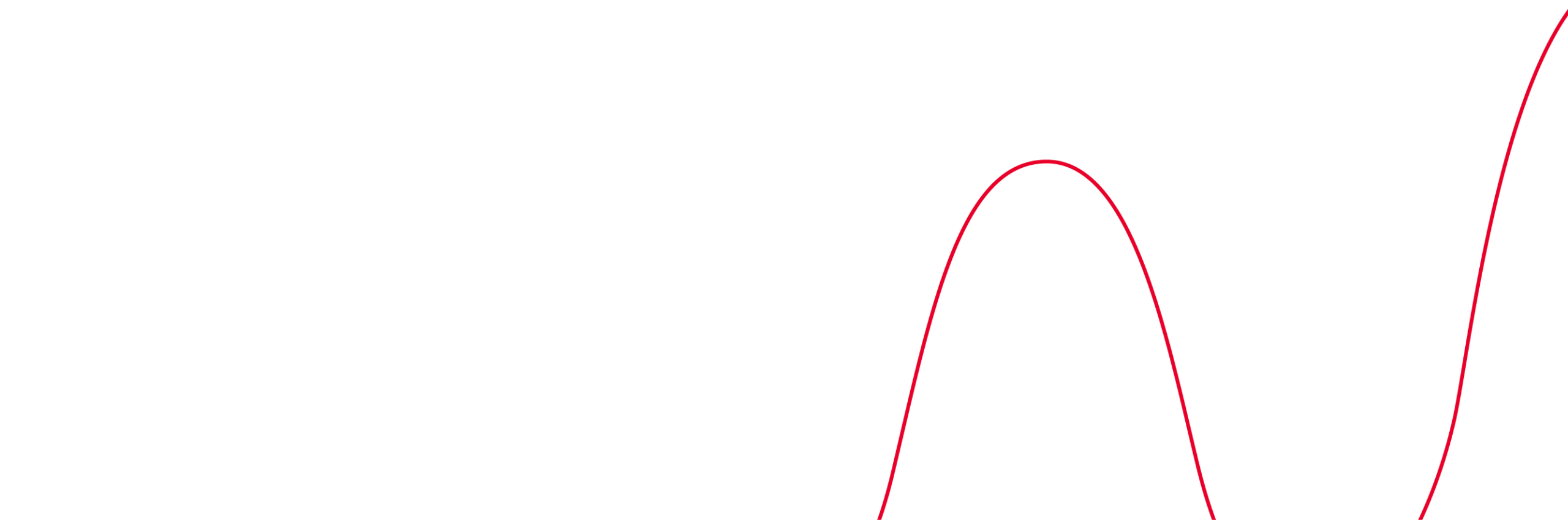
Summary of Supported Memory Interfaces

Best design platform for Memory Systems



One Tool, Multiple Standards Covered!

SerDes Design Workflow

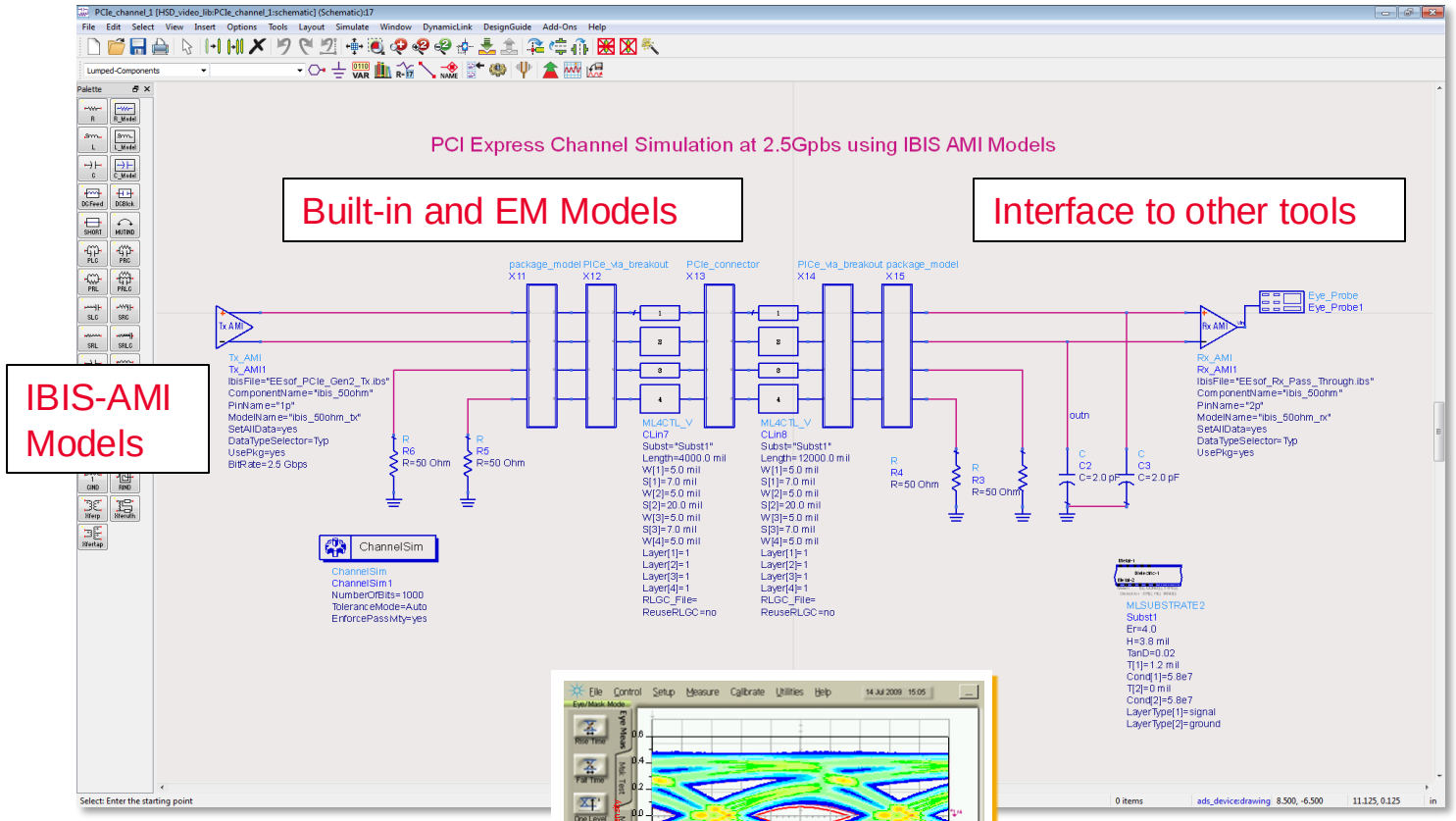


SerDes Design Workflow

High-Speed Channel Simulation enables Chip-to-Chip Link Analysis

Key Takeaway
Keysight ADS covers multiple SerDes applications

- ADS's Channel simulation enables complete chip-to-chip link analysis
- IBIS-AMI Modeling supported (PCIE5 AMI Modeler, USB4 AMI Modeler, etc)
- Verify high speed digital signal and power integrity design for standards like PCI Express®, Ethernet, DDR, HDMI, USB and SATA.



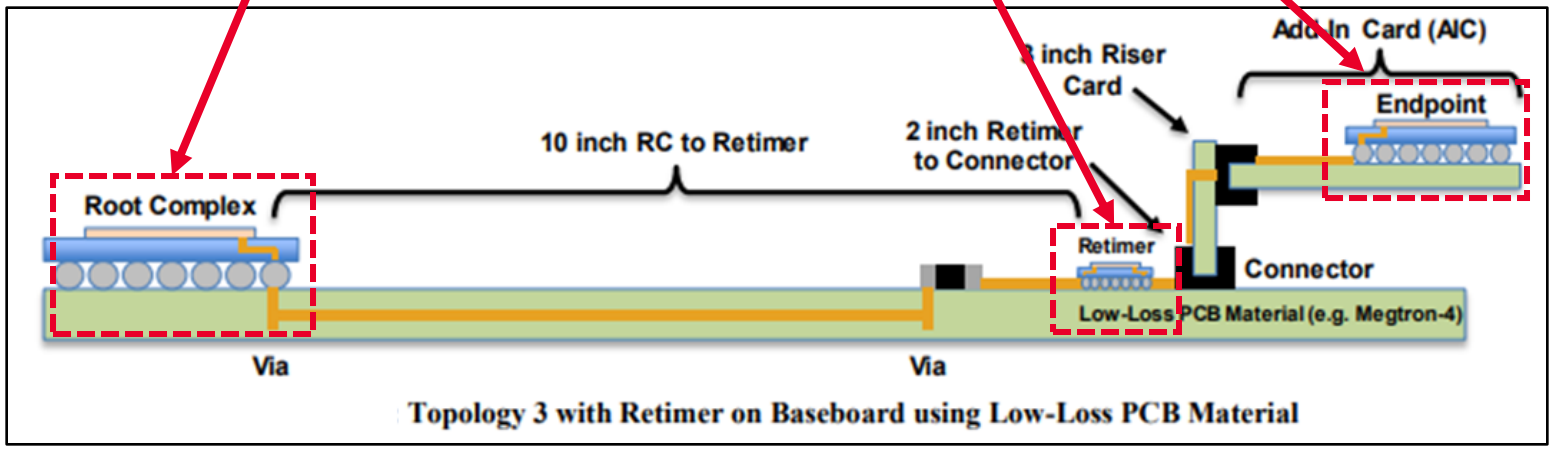
Measured vs. Modeled Eye Diagrams

What Matters in PCIe Simulations?

Simulator, Chipset Models, Channel models

For Root Complex, Retimer, Endpoint

1. **IBIS Models**
   (Input/Output Buffer Information)
2. **IBIS-AMI Models**
   (Algorithmic Modeling Interface)
3. **HSPICE Models**



Root Complex
- Interface between CPU, Memory and the rest of PCIe Interface

Retimer
- Compensate loss at high data rate
- Recovers timing of bits received and retransmits the bit sequence

Endpoint
- PCIe End Component/Devices (E.g SSD, GPU)

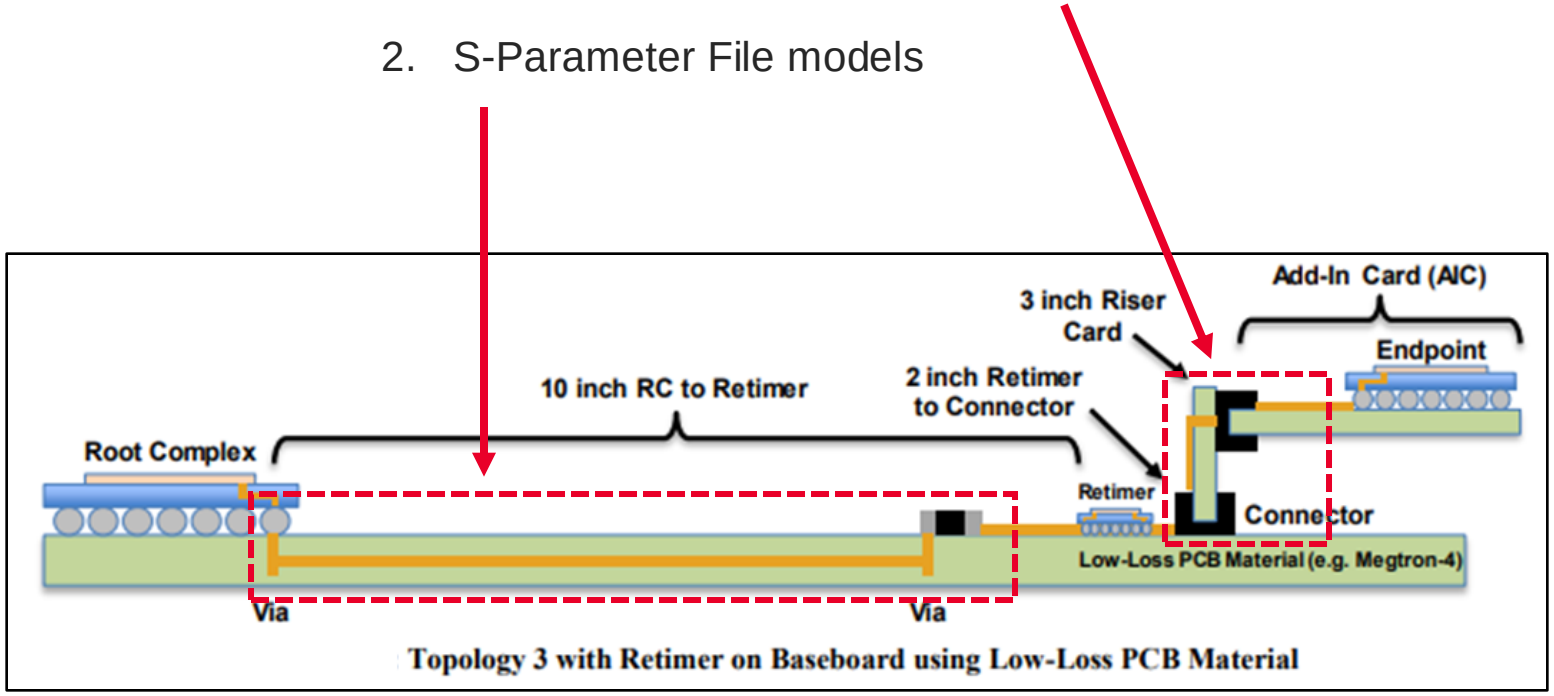
What Matters in PCIe Simulations?

Simulator, Chipset Models, Channel models

RC to Retimer/Retimer to Endpoint Channel

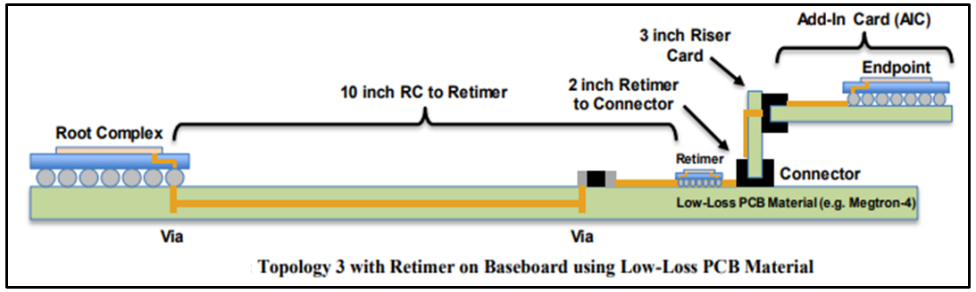
Pre- and Post-Layout Channel Models

1. EM Simulation Models
2. S-Parameter File models

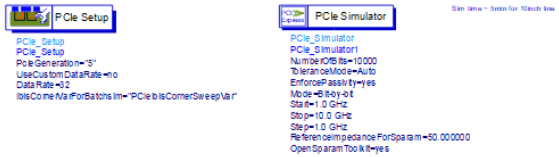


System Designer for PCIe®

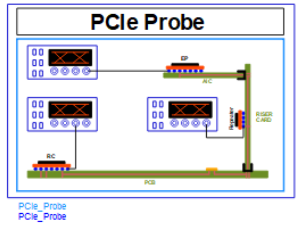
A smarter design workflow for PCIe applications

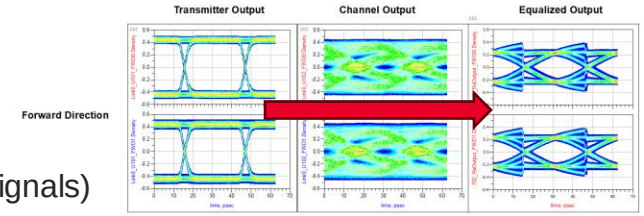


- Streamlined design and simulation workflow for PCIe applications, Gen5 and Gen6 (PAM4)
  - Supports multi-links and multi-lanes PCIe system
  - PCIe_RootComplex, PCIe_EndPoint, PCIe_Repeater, PCIe_Simulator, PCIe_PreLayout, PCIe_PostLayout, PCIe_Tline, PCIe_Probe, PCIe_Compliance_Probe, and PCIe_Setup
- Dedicated PCIe simulator
- Supports Seasim Interface
- Included PCIe Compliance Tests
- Included PCIe AMI model builder



PCIe Probe
(measurements: groups of signals)



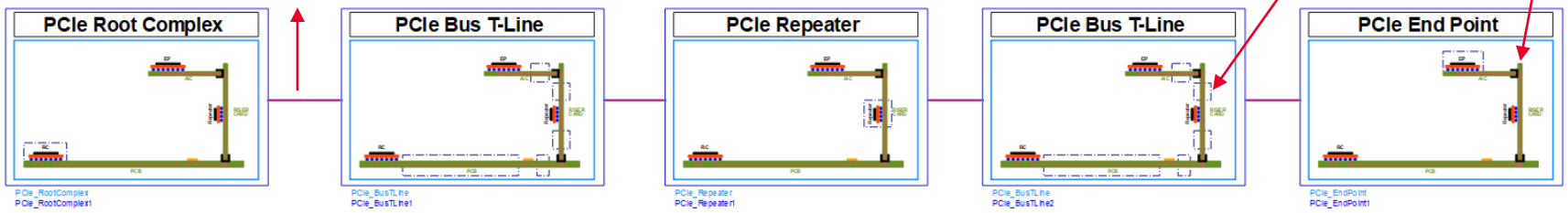


Smart Bus Wire
(One click connection)

10 Inch Transmission Lines

10 Inch Transmission Lines

Smart Components
(Easy model setup)

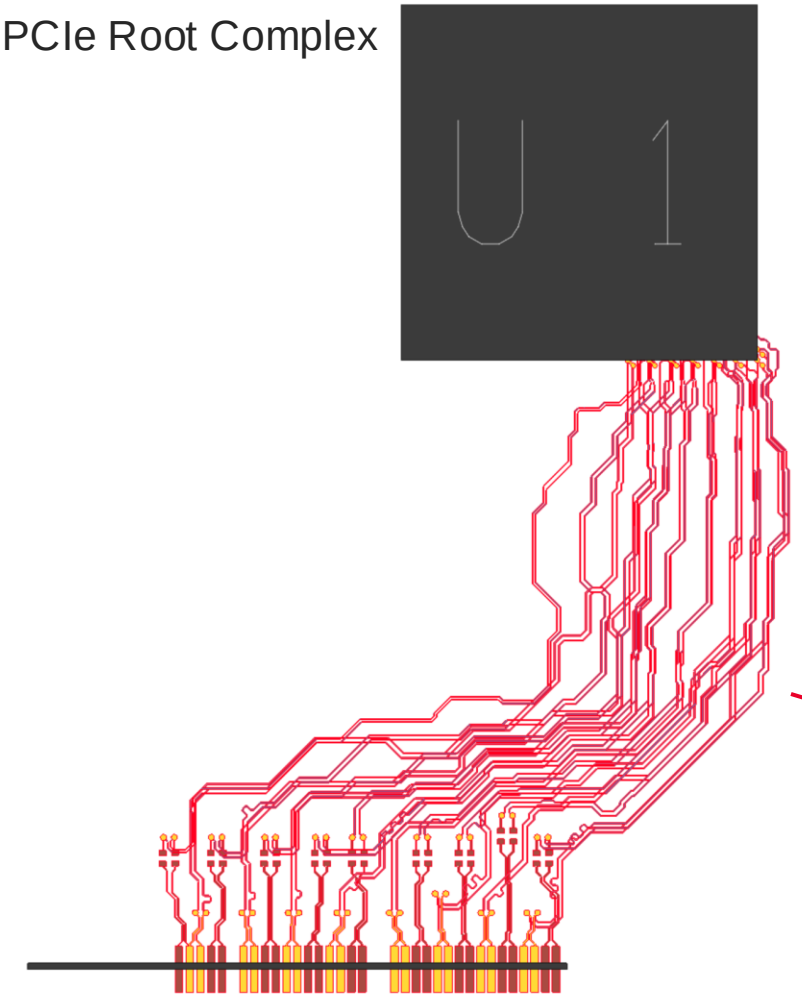


Example – Byte1 (DQ0~DQ7,DQS0 and DM0) on Platform Board

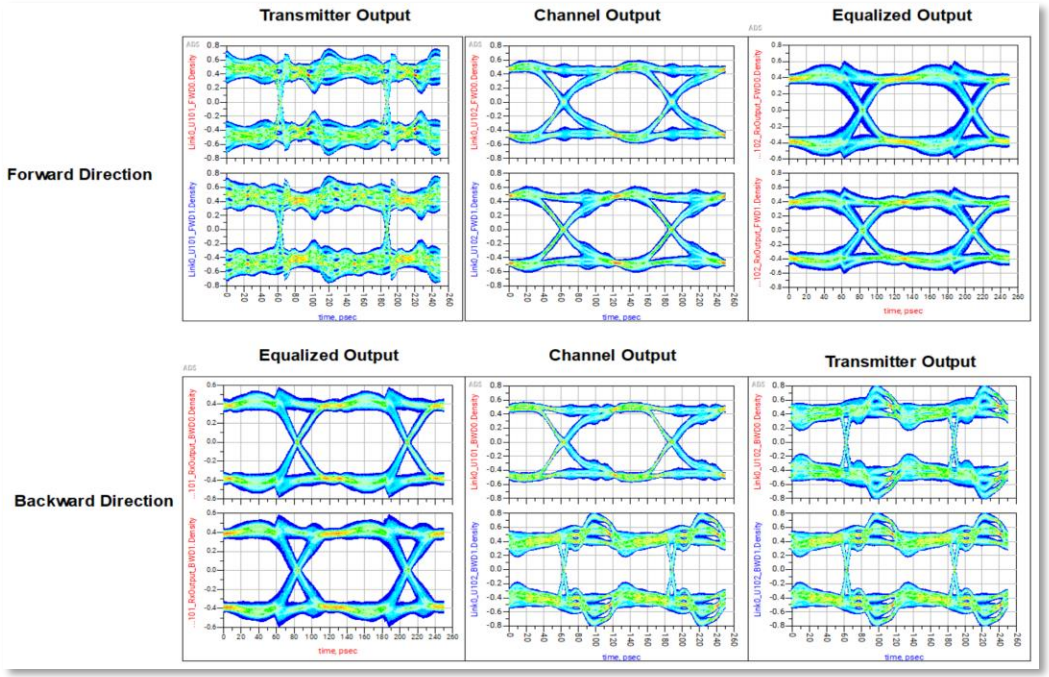
Simulation Structure, Setup, and Results

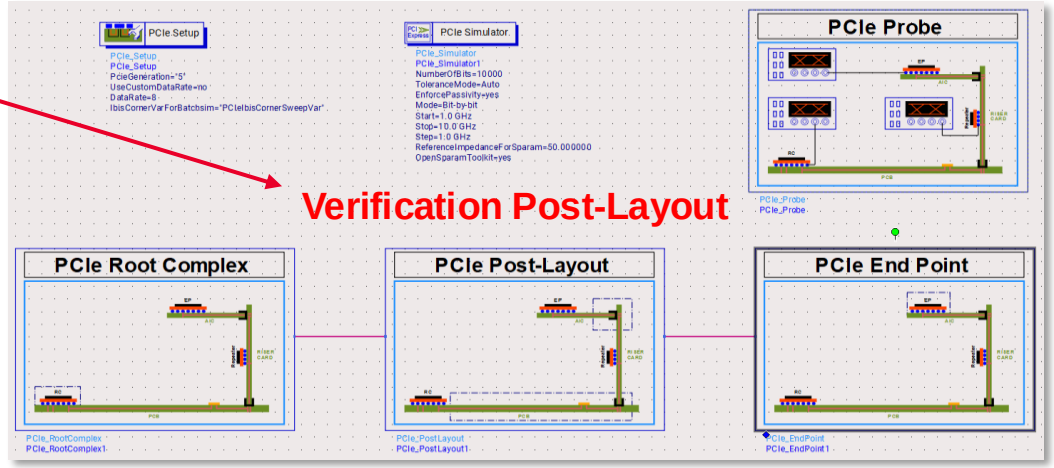
With 3D EM Model (SIPro)

PCIe Root Complex



PCIe End Point

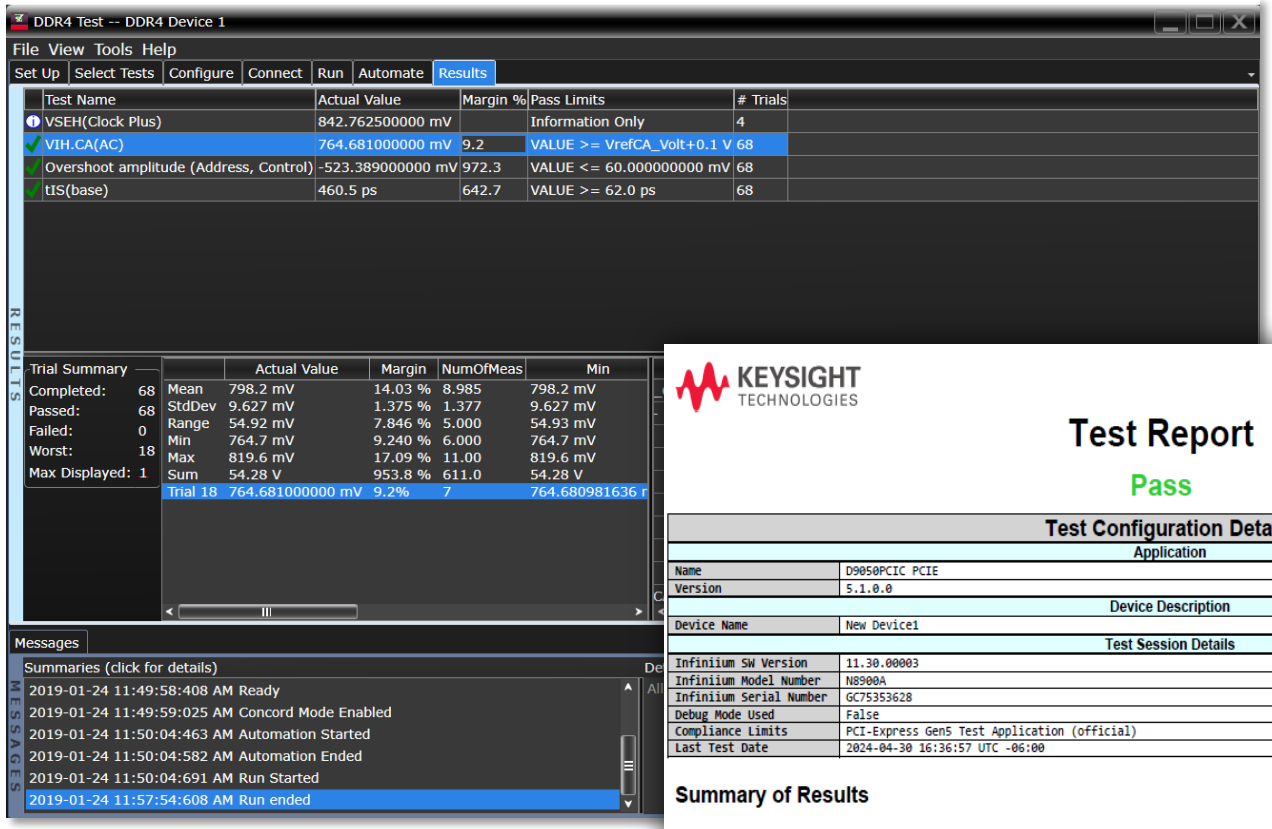


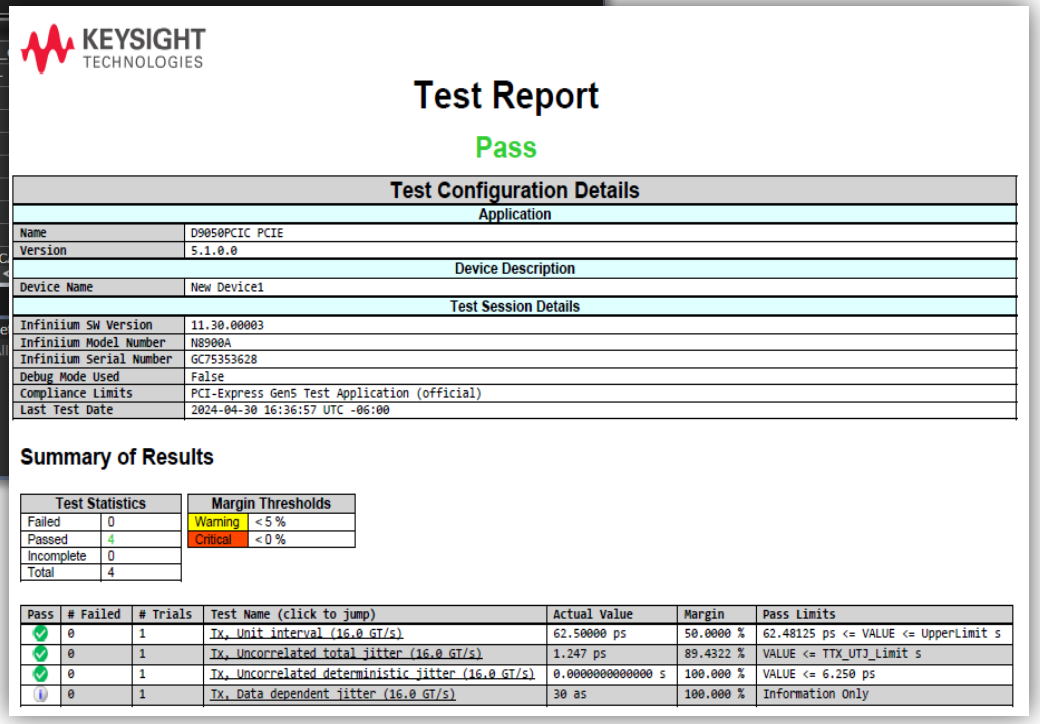


KEYSIGHT

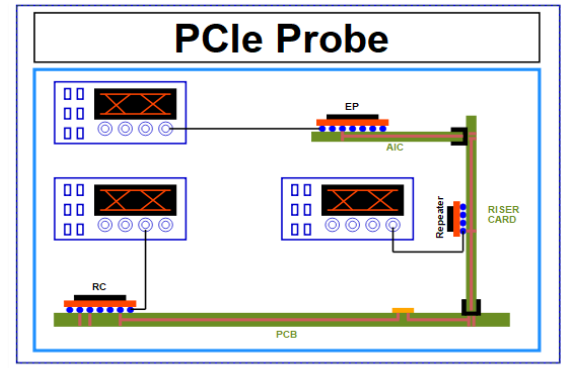
Investigate Pre-Compliance for Sign-Off

Industry proven measurement science

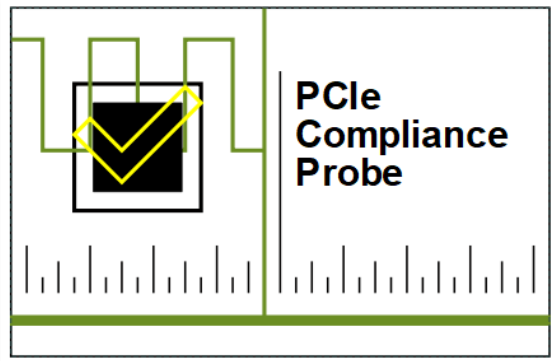




Automatically invoked and controlled by ADS



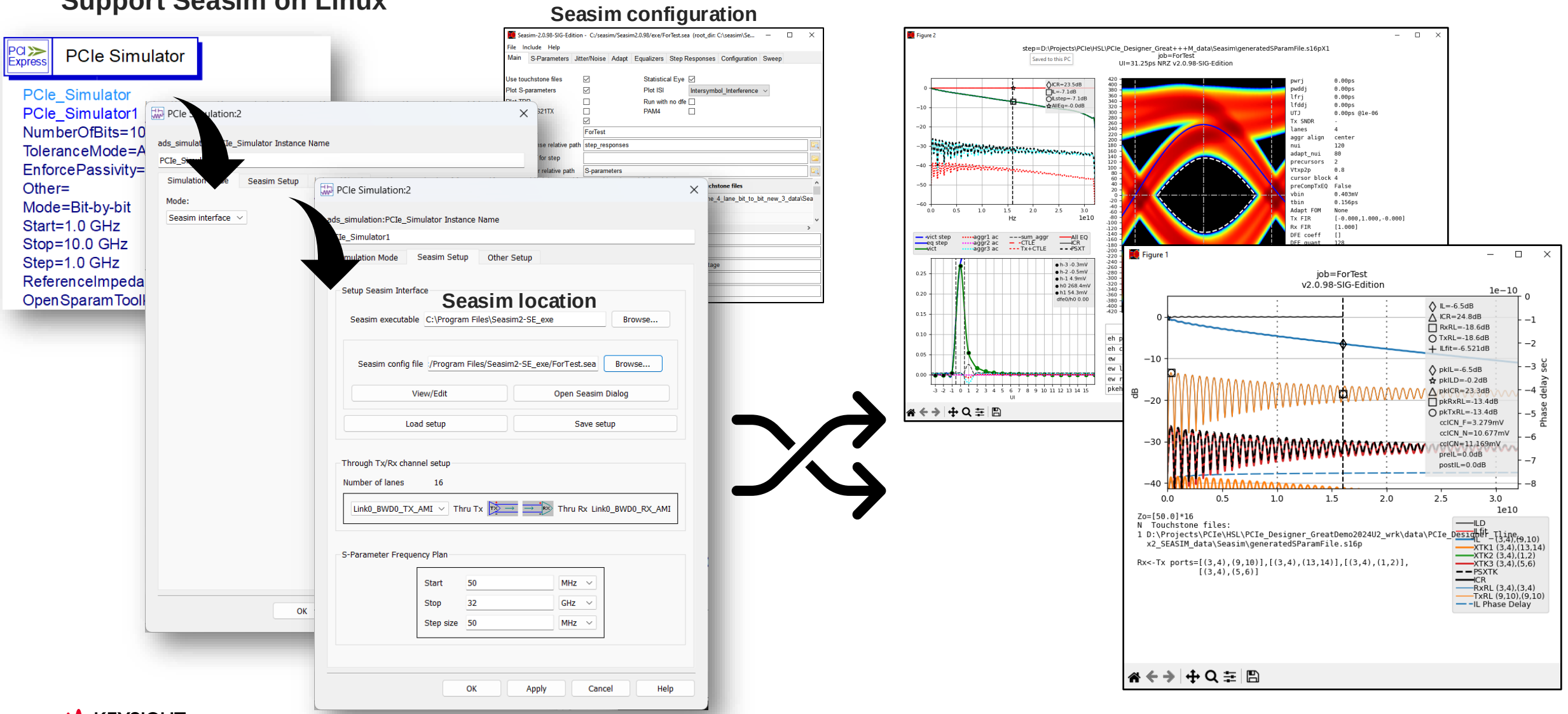
PCIe_Probe
PCIe_Probe



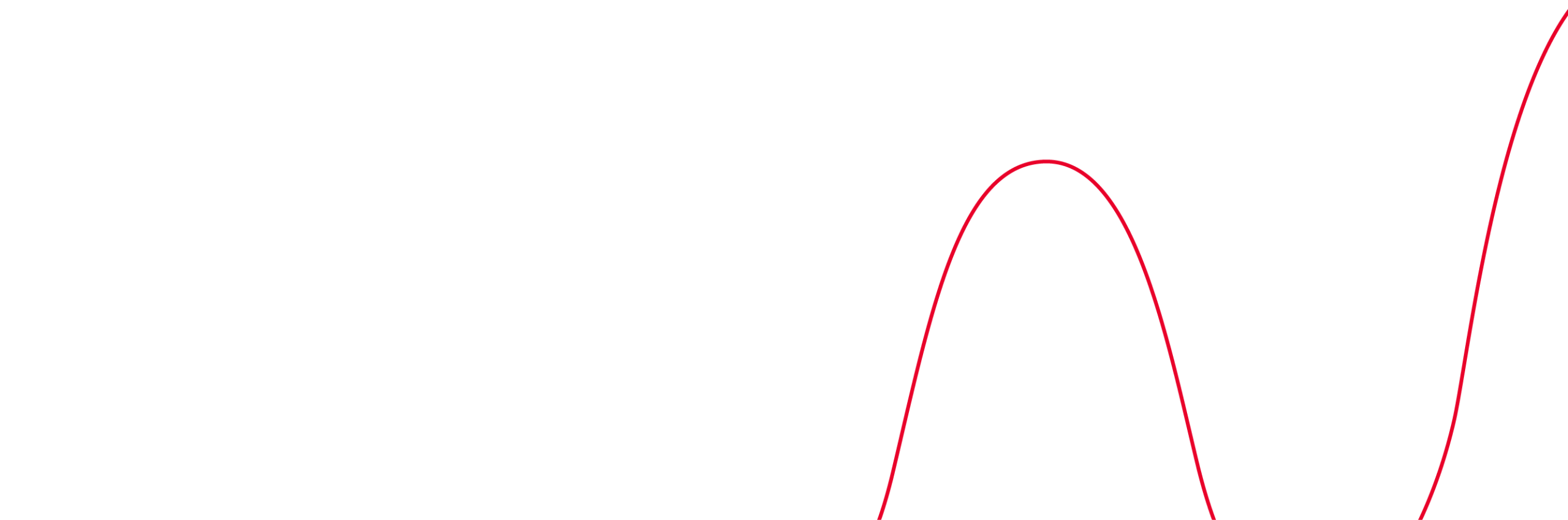
PCIe_Compliance_Probe
PCIe_Compliance_Probe

Seasim Interface for System Designer for PCIe® (W3651B)

Support Seasim on Linux



Conclusion

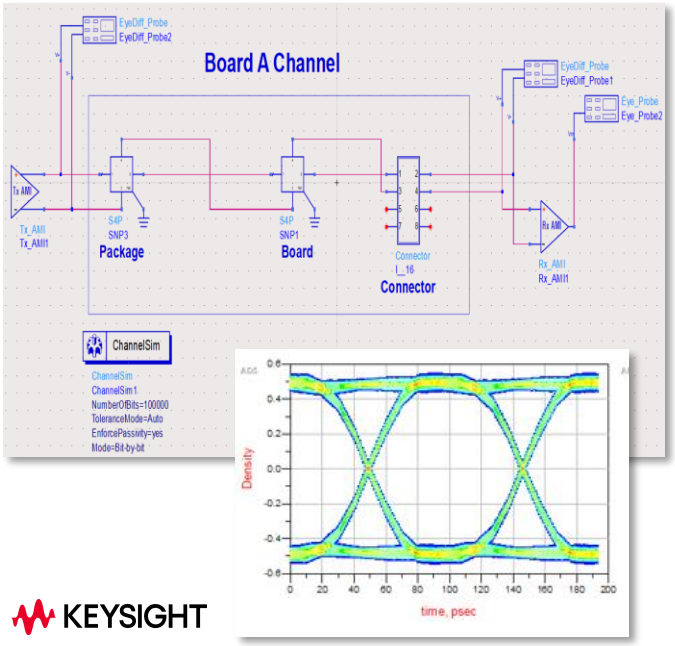


ADS HSD Design Flow

ADS accelerate High-Speed Digital Workflows

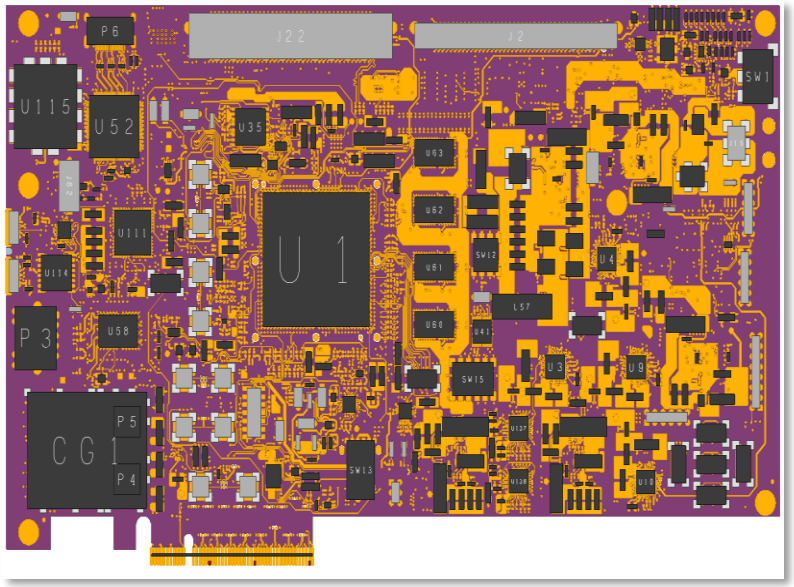
Pre-Layout

Pre-investigation of channel performance



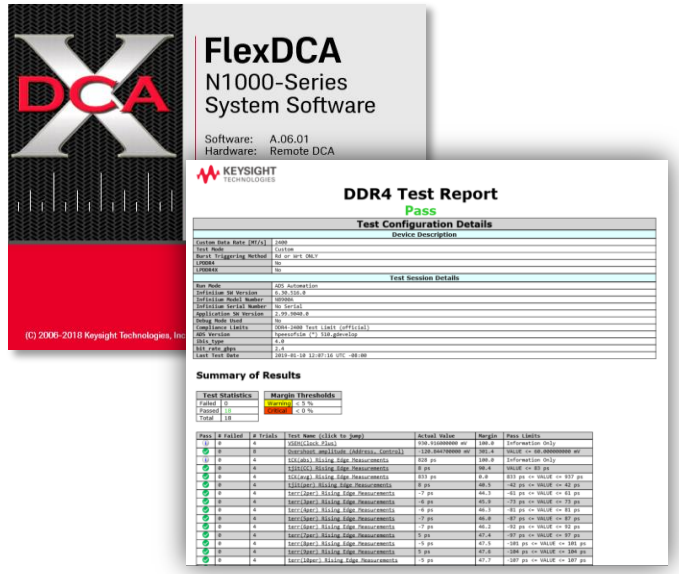
Post-Layout

EM simulation of Design for Signal and Power Integrity



Verification/Measurement

Verification of Design with Compliance Test Benches and Instrument measurements



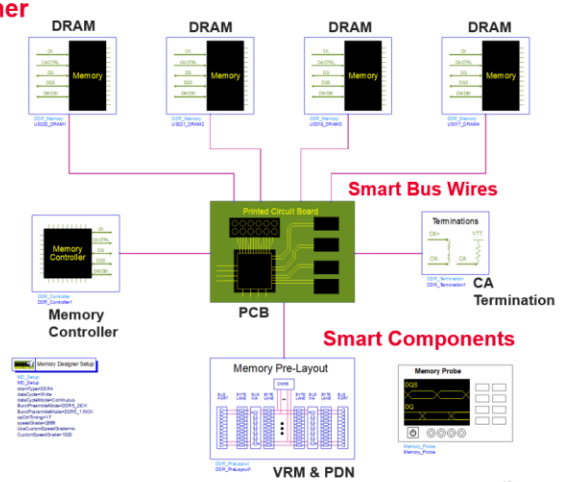
Conclusion

Smart Workflow for Efficient and Accurate Designs

PathWave ADS Memory Designer

- Simulation Environment designed with the Memory Design Engineer in mind
- Smart bus, components, and Memory Eye Probe
- Multiple Simulation Engines
  - Transient Convolution
  - DDR BUS Sim
    - Bit-by-Bit Simulation
    - Statistical Simulation
- Compliance Report Generation
- Single-Ended PAM-4 simulation capability
- IBIS-AMI model generation wizard
- CA Data Bus Designer
- DDR extraction wizard in SIPro

and much more…

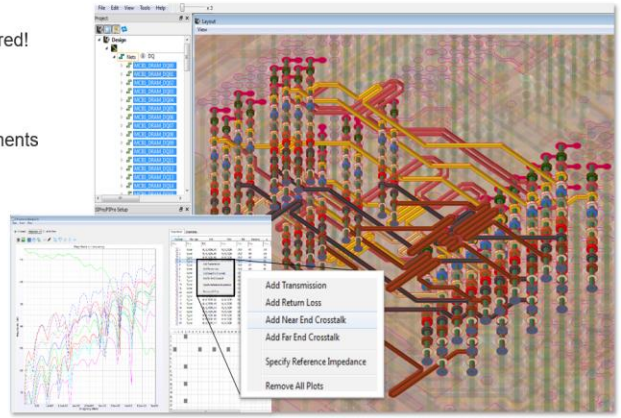


KEYSIGHT 16

SIPro Electromagnetic PCB Extraction

Layout to results in less than 20 clicks

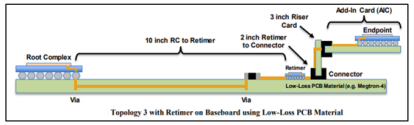
- No layout simplification required!
- Net-driven
- Guided port creation
- Quickly plot all crosstalk elements from the same component
- Easily plot TDR/TDT
- Mixed-mode S-parameters
- One-click schematic generation



KEYSIGHT 8

System Designer for PCIe®

A smarter design workflow for PCIe applications



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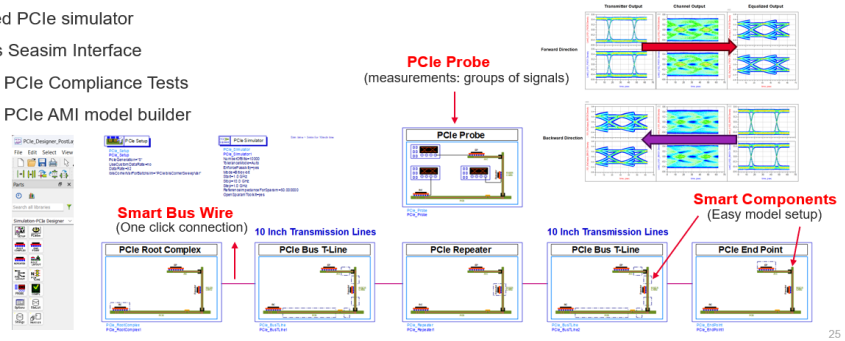

KEYSIGHT 25


KEYSIGHT